LOAD COMPENSATION AND VOLTAGE REGULATION OF DISTRIBUTION SYSTEM USING DSTATCOM

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to the

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CERTIFICATE

This is to certify that the work contained in the thesis entitled "**Load Compensation and Voltage Regulation of Distribution System using DSTATCOM**" by Mahesh Kumar has been carried out under our supervision and this work has not been submitted elsewhere for a degree.

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Dedicated to

my family

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Thesis Title	:	**LOAD COMPENSATION AND VOLTAGE REGULATION OF DISTRIBUTION SYSTEM USING DSTATCOM**

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SYNOPSIS

There has been a significant increase in the use of consumer electronics requiring switched mode power supplies and power electronic devices such as adjustable speed drive in the last couple of decades. These have caused a serious problem of harmonic pollution in power distribution systems. The excessive harmonic current in the network causes voltage distortion, excessive neutral current flow, heating of electrical machines and transformers and poor power factor. Therefore, cleaning up the supply power is a challenging proposition. This has led to the evolution of various load compensation techniques.

In the most primitive form of load compensation, passive LC filters were used. But passive LC filters have certain problems. They may create new series or parallel resonance. The number of passive filters required are same as the number of harmonics in the load currents to be eliminated. To overcome these problems associated with passive filters, active power filters were evolved by eminent researchers in 1970s. With the improvement in switching characteristics of power semiconductor devices, e.g. IGBTs, GTOs and their voltage and current rating, active power filter technology grew consistently. These filters are currently regarded as the most efficient option to solve

problems created by non-linear loads. The sophisticated PWM inverter technology and the recently developed control algorithms helped the active power filters to reach the stage of commercial installations.

In 1978, sampling and averaging techniques of load compensation were proposed by Gyugyi et al. [1]. These methods of load compensation can only supply the fundamental reactive power of the load. However, they are not suitable for time varying and/or non-linear loads. Out of many methods for generating the compensator reference currents, the *pq* theory has gained considerable attention and is well established [2].

The compensation scheme based on the *pq* theory can eliminate all unbalances and harmonics caused by non-linear time varying load provided source voltages are balanced and sinusoidal and power converter has sufficient bandwidth to track the reference compensator currents. However when the source voltages are unbalanced, the scheme does not provide satisfactory results. Furthermore, reference current generation scheme is computation intensive due to $\alpha\beta 0$ and inverse $\alpha\beta 0$ transformations. On the other hand, load compensation based on theory of instantaneous symmetrical components [3] is much simpler than *pq* theory. It does not require complex transformations of currents and can effectively control the phase angle of the source currents.

The compensation based on generalized instantaneous reactive power theory [4-5] is much more general. In this, the instantaneous compensator current includes both the active and reactive power components. Nevertheless formulating reference current vector in terms of compensator powers makes the choice for compensator powers more difficult and indirect.

To realize the active shunt power filters, various distribution static compensators (DSTATCOM) topologies are used. A DSTATCOM consists a three-phase voltage source inverter (VSI) that are driven by dc storage capacitor(s). The output of the VSI is connected to the ac system through three interface inductors or transformers. The point at which this connection is made is called the point of common coupling (PCC). For instance in [3] a single dc storage capacitor and three single-phase inverter with isolation transformers are used to realize active shunt power filter. In cases where the load contains dc current, the compensator must cancel it such that the current drawn from the source is

a pure sinusoid. In this case, topology presented in [3] will fail. Neutral clamped inverter topology [6] in which two dc capacitors supply the voltage source inverter (VSI) is not very effective for loads containing ac and dc components. The dc component of the current has a tendency to charge one capacitor and discharge the other. A three-phase, four-leg inverter with single dc storage capacitor topology [7] can be used for ac and dc load compensation, but it passes inverter switching components to the system neutral.

The algorithms used for generating reference currents usually assume that voltage at PCC is stiff. However, distribution loads are generally supplied through feeder. Thus if these algorithms are used for the generation of reference filter currents, it results into erroneous compensation as switching frequencies of the inverter are passed to the voltages at PCC. Since these shunt algorithms assume balanced voltages, taking the distorted PCC voltage as an input to these algorithms results in distortion of source current too.

The use of a DSTATCOM for load compensation is very common. In this, the DSTATCOM compensates for the unbalance and distortion in the load current by injecting current to cancel these effects. In this thesis, this is termed as the operation of DSTATCOM in current control mode. The DSTATCOM is however, is much more flexible device that can also be used for controlling the voltage of a distribution bus against any distortion. This is termed as the operation of DSTATCOM in voltage control mode.

Keeping in view the above considerations, we define the following objectives of the thesis:

1. To evolve a general algorithm for various kinds of shunt compensation schemes.
2. To find a suitable topology which works for compensation of load currents with ac and dc components under balanced and unbalanced voltages.
3. To provide a control algorithm for load compensation when the source is not stiff.
4. To provide DSTATCOM control to regulate the bus voltage at a nominal value.

Research has been carried out to achieve the above mentioned objectives and the major contributions of the thesis are:

1. A shunt algorithm is proposed based on generalized instantaneous reactive power theory [4]. This is called the generalized theory as all other theories e.g. *pq* theory [2], theory of instantaneous symmetrical components [3] can be derived from it. By appropriate selection of source power terms, we can obtain different kinds of compensation [8]. The general algorithm is then modified for load compensation under unbalanced source voltages. The feasibility of shunt algorithm is demonstrated by realizing DSTATCOM using neutral clamped inverter. Its performance is studied both in steady state and transient conditions. It is shown that the compensator exhibits the fast dynamic performance.

2. It is illustrated that when the load currents contain dc components in addition to ac components, voltage imbalance occurs with neutral clamped inverter that leads to erroneous compensation. To overcome this problem, a new DSTATCOM topology is proposed [9] in which a chopper circuit is connected to the neutral point of the dc capacitors. Various control schemes of chopper are proposed to regulate the voltage of the dc capacitors around a reference value. This ensures the correct performance of the compensator for load currents containing dc component.

3. To overcome the voltage distortion problem when the source voltage is not stiff, fundamental of the PCC voltages is extracted and fed to the shunt algorithm. In addition, a state feedback hysteresis band controller is used for tracking control signal. An interesting feature of this control is that the inverter switching frequency components are highly attenuated in source current and the PCC voltage. It is demonstrated that for balanced and sinusoidal upstream source voltage, the proposed control gives excellent performance. The control scheme also produces satisfactory performance when the upstream source voltage is distorted.

4. An algorithm to operate DSTATCOM in voltage control mode is suggested which regulates the bus voltage at a nominal value. A dead-beat control for switching of the inverter is used. The DSTATCOM in this mode is able to maintain the PCC voltage

balanced and distortion free irrespective of distortion either in the source or the load side.

OUTLINE OF THE THESIS

Chapter 1 introduces the concept of load compensation and voltage regulation using DSTATCOM. A detailed literature review is also presented.

Chapter 2 begins with the discussion on general theory of shunt compensation. Various shunt compensation theories, i.e., sampling and averaging techniques, source current synthesis using capacitor voltage feedback, *pq* theory, load compensation using instantaneous symmetrical component theory and generalized instantaneous reactive power theory are described. It is shown that different compensation requirements can be satisfied with the generalized instantaneous reactive power theory. The general shunt algorithm is then modified for systems with unbalanced source voltages. All the above algorithms are verified through detailed simulation and experimentation with an ideal inverter.

In **Chapter 3**, various DSTATCOM topologies are described to realize shunt compensator for ac load compensation. Neutral clamped inverter topology is chosen for ac load compensation in the three-phase, four-wire distribution systems. The control loop for dc capacitors voltage is described. The state space model of the compensator is developed. The voltage source inverter is operated in a hysteresis band current control mode. Based on the state space model, the simulation results for the steady state and the transient performance of the compensator are presented. The balanced as well as unbalanced source voltages are considered. The simulation results are also verified through experiments.

A new DSTATCOM topology called neutral clamped inverter-chopper topology is proposed for compensation of loads with ac and dc components in **Chapter 4**. It is compared with other existing topologies. Due to the presence a dc component in the load current, the dc capacitors face voltage imbalance problem i.e., one capacitor discharges while the other charges uncontrollably. To solve this imbalance problem, a chopper

circuit is used. Various chopper control schemes are presented and they are verified through simulation. Some of the selected schemes are also verified through experiments.

In **Chapter 5**, load compensation with non-stiff source is considered. It is demonstrated that if any of the shunt algorithms for stiff voltage source is applied to a system with non-stiff voltage source, the PCC voltage gets distorted. To eliminate these distortions, a positive sequence voltage extraction algorithm is used and reference compensator current is calculated using the shunt algorithm described in Chapter 2. These are used to form the reference state vector. A state feedback switching controller is then designed for tracking the reference state vector. This guarantees that the PCC voltages as well as the source currents are perfectly balanced and sinusoidal. Thus in addition to the load compensation the compensator also improves the terminal voltage and makes it distortion free. However, source currents may not remain balanced and sinusoidal when upstream source voltages are unbalanced and contain harmonics. All the above points are demonstrated through digital simulation and experimental results.

DSTATCOM that operates in voltage control mode to regulate the voltage of PCC is designed in **Chapter 6**. The magnitude of the PCC voltage can be arbitrarily chosen while its phase angle is obtained by the dc capacitor voltage control loop. This control loop ensures that source supplies the active power to the load and losses in the inverter. It is demonstrated that under unbalanced and distorted source voltages and load currents, the PCC voltage is regulated at the nominal value. Detailed simulation and experimental results are also presented.

The thesis ends in **Chapter 7** where, the general conclusions derived from the thesis are presented and some scope for future work is suggested.

The experimental set up used in the laboratory is given in the Appendices.

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v_{sa}, v_{sb}, v_{sc}	Source voltage of phases *a*, *b* and *c* respectively
i_{sa}, i_{sb}, i_{sc}	Source current in phases *a*, *b* and *c* respectively
i_{la}, i_{lb}, i_{lc}	Load current in phases *a*, *b* and *c* respectively
v_{ta}, v_{tb}, v_{tc}	Terminal voltage of phases *a*, *b* and *c* respectively
i_{fa}^{*}, i_{fb}^{*}, i_{fc}^{*}	Reference compensator (filter) currents in phases *a*, *b* and *c* respectively
i_{fa}, i_{fb}, i_{fc}	Actual filter compensator current in phases *a*, *b* and *c* respectively
K_p, K_i	Proportional and integral gains of PI controller
v_α, v_β, v_o	Voltages in $\alpha\beta 0$ domain
i_α, i_β, i_o	Currents in $\alpha\beta 0$ domain
p, q	Three phase instantaneous active and reactive power respectively
$\bar{p}$, $\bar{q}$	Average values of active and reactive power respectively
$\tilde{p}$, $\tilde{q}$	Zero mean oscillating active and reactive powers respectively
$\bar{p}_l$, $\bar{q}_l$	Average load active and reactive power respectively
p_o	Zero sequence power
P_{loss}	Losses in the inverter
v_{a0}, v_{a1}, v_{a2}	Zero, positive and negative sequence instantaneous symmetrical components of three-phase voltages v_a, v_b, and v_c respectively
i_{a0}, i_{a1}, i_{a2}	Zero, positive and negative sequence instantaneous symmetrical components of three-phase currents i_a i_b and i_c respectively
$\boldsymbol{v}$, $\boldsymbol{i}$	Instantaneous voltage and current in vector form
$\boldsymbol{q}_{abc}$, $\boldsymbol{q}_{\alpha\beta 0}$	Instantaneous reactive power in vector form in *abc* and $\alpha\beta 0$ domain respectively
C_1, C_2	DC storage capacitors supplying a VSI

v_{c1}, v_{c2}	Voltage across dc capacitors C_1 and C_2 respectively
N, n, n'	System, load and compensator neutral respectively
S_j, $\bar{S}_j$	Status of inverter switches in phase-j for $j = a, b, c$
S_l, S_u	Status of chopper switches
R_{ch}, L_{ch}	Chopper resistance and inductance
i_{ch}	Chopper current
$i_{ch\ limit}$	Current limit for chopper
$i_{ch\ \max}$	Maximum chopper current
t_{7on}, t_{7off}	ON and OFF times of chopper switch S_7
t_{8on}, t_{8off}	ON and OFF times of chopper switch S_8
D	Duty cycle of chopper
R_s, L_s	Feeder resistance and inductance respectively
C_{fa}, C_{fb}, C_{fc}	AC filter capacitors in phases a, b and c respectively
i_{cfa}, i_{cfb}, i_{cfc}	Filter capacitor currents in phases a, b and c respectively
v_{cfa}, v_{cfb}, v_{cfc}	Filter capacitor voltages in phases a, b and c respectively
$\boldsymbol{x}$, z	State vectors
z_{ref}	Reference state vector
$\boldsymbol{Q}$, R	LQR weighting matrices
J	Performance index
lim	Control signal hysteresis band
ϕ	Phase angle between source voltage and source current
	State transition matrix
θ	Input matrix
δ	Power angle
p_{sh}	Instantaneous shunt power
P_{sh}	Shunt power averaged over each cycle

P_{shref}	Reference shunt power
K_{pv}	Proportional gain for voltage dc capacitor loop
$K_{p\delta}$, $K_{i\delta}$	Proportional and integral gains of PI δ control loop

CHAPTER 1

INTRODUCTION

In the last couple of decades, there has been tremendous increase in consumer electronics and usage of electronic power devices in industries. The power electronic devices such as cyclo-converters in steel mill drives, arc furnaces, arc welding machines, static converters, (i.e. diode rectifiers, thyristor controlled rectifiers, half wave rectifiers) cause severe harmonic pollution in power systems. Various power electronic based loads such as switched mode power supply and UPS, microwave ovens, laser printers, medical instrumentation, electric lighting and other electronic equipment also cause serious harmonic pollution. Other than balanced loads that draw purely sinusoidal currents, there are many loads that are unbalanced. In addition, there are power electronic loads that draw harmonic currents. Usually these loads are non-linear. The loads that draw unbalanced and harmonic currents can be classified as,

- Unbalanced ac sinusoidal load currents
- Unbalance ac non-sinusoidal load currents containing fundamental and harmonics
- Unbalance non-sinusoidal load currents containing ac and dc

The harmonic pollution caused by these non-linear loads has been a serious problem. Some of the adverse effects of non-linear loads are:

- Voltage distortion
- Excessive neutral return current
- High levels of neutral to ground voltage
- Overheating of electric machines and transformers

In addition there may be balanced loads that have poor power factor. These are the matters of serious concern both for the customers and the utility. On the other hand, the demand for clean power supply is growing for sensitive loads such as computers, medical

electronic equipment and automated processes. This demand has led to the evolution of various load compensation techniques.

The most primitive scheme of load compensation has been the use of passive LC filters. Passive filters consisting of tuned LC filters have been traditionally used to absorb the harmonics in the power system because of their simplicity, low cost and high efficiency. The LC filters are connected in parallel with a harmonic current generating load. A tuned LC filter should be designed to exhibit lower impedance at tuned frequency and higher impedance at the supply (fundamental) frequency. In principle, filtering characteristics of a passive filter are determined by the impedance ratio of the Thevenin source impedance and the impedance of the passive filter. Therefore, it is difficult for a passive filter installed in the vicinity of a harmonic producing load to meet the above design criteria. In addition the passive filters have following problems [1-3]:

- The application of passive tuned filters creates new system series and parallel resonance.
- Passive filters may also absorb the power at frequencies other than that for which they are tuned.
- Passive filter ratings needs to be coordinated with the reactive power requirements of the loads.
- A separate passive filter is installed for each of the harmonics to be compensated.

To overcome the aforesaid problems, active power filters have been proposed by researchers. In 1970's, their basic principles were discussed [4-6]. However there was almost no progress in active filters beyond the laboratory testing stage, since at that time the power electronic device technology was not sufficiently advanced to implement the compensation principles practically. Recent progress in voltage and current rating and switching speed of semiconductor power devices such as IGBTs, GTO thyristors has spurred interest in the study of active power filters with a focus on practical applications. Sophisticated PWM inverter technology along with the recently developed control algorithms has made it possible to put them into some commercial installations.

1.1 ACTIVE POWER FILTERS

Due to harmonic-related problems in utility and industrial power system, active power filters have attracted great attention. Active power filters use power electronics to produce harmonic components that cancel the harmonic components of the non-linear loads. The active power filter includes a power converter and a control loop, which controls the harmonic injection of the filter into ac network, based on load harmonics. The load currents and terminal voltages are sensed and measured continuously. Based on these measurements, the harmonic currents are injected into the ac system to cancel the load current harmonics. Some of the benefits using active power filter are:

- They are capable of removing wide range of harmonic frequencies and not just characteristics harmonics.
- They can reduce or even eliminate neutral current in a three-phase, four-wire system.
- Active filters adapt to changes in load as they happen.
- They are generally smaller in size compared to passive filters.
- They also add damping to the network.
- They can correct power factor.

1.2 CLASSIFICATION OF ACTIVE POWER FILTERS

Active power filters may be classified on the basis of the power circuit (converter type) used for realizing the active filter, the connection topology or on the type of the supply system [2, 7-8]. These are discussed below.

1.2.1 Classification Based on Converter type

Two types of power converter circuits are used in active power filters

- Voltage source inverter (VSI)
- Current source inverter (CSI)

VSIs have an input dc bus with a sufficiently large dc capacitor or dc supply. This configuration is widely used because it is lighter, cheaper and expandable to multi-level

inverter versions for enhancing the performance at high power levels with lower switching frequencies [9-11]. This is popularly used in UPS also.

CSIs behave as nonsinusoidal current sources to meet harmonic current requirements of the nonlinear loads [12-14]. These inverters are more reliable and fault tolerant than VSIs. They have higher losses and are difficult to use in multi-level or multi-step mode to improve the performance in the higher power ratings.

Use of hybrid structure of energy storage in converter has also been reported in literature [15]. It uses both inductive and capacitive elements together. Through suitable logic, the two energy storage elements are interfaced. As regards energy storage capacitive elements are far more efficient, smaller and less expensive than inductive ones, except in cases where very large amount of energy storage is required. In such cases, super-conductive inductors can be used [12]. Voltage source inverter is however preferred over the current source inverter topology, because the voltage source inverter is higher in efficiency and lower in initial cost than the current source inverter [2]. Multi-level VSIs topologies are also suitable for static VAr compensator [9] as they allow lower inverter switching frequency, minimize device stresses in high power applications.

1.2.2 Classification Based on Topology

On the basis of topology the active filters can be classified as

- Shunt active power filter
- Series active power filter
- Series active and shunt passive power filter (hybrid power filter)
- Unified power quality conditioner (UPQC)

Fig. 1.1 (a)-(d) shows the above topologies. They are briefly described below.

Shunt active power filter

This configuration is widely used for eliminating the current harmonics due to nonlinear loads. It is mainly used at load distribution centers. The active shunt power filter shown in Fig. 1.1 (a), is one of the most commonly used configurations. The compensator is

connected in parallel with the nonlinear load. The point that joins the shunt filter with the ac system is called the Point of Common Coupling (PCC). The aim of the compensator is to inject the harmonic currents to cancel out the harmonics of the load [16-20]. The dc storage capacitors are used to support the operation of voltage source inverter (VSI) in current control mode.

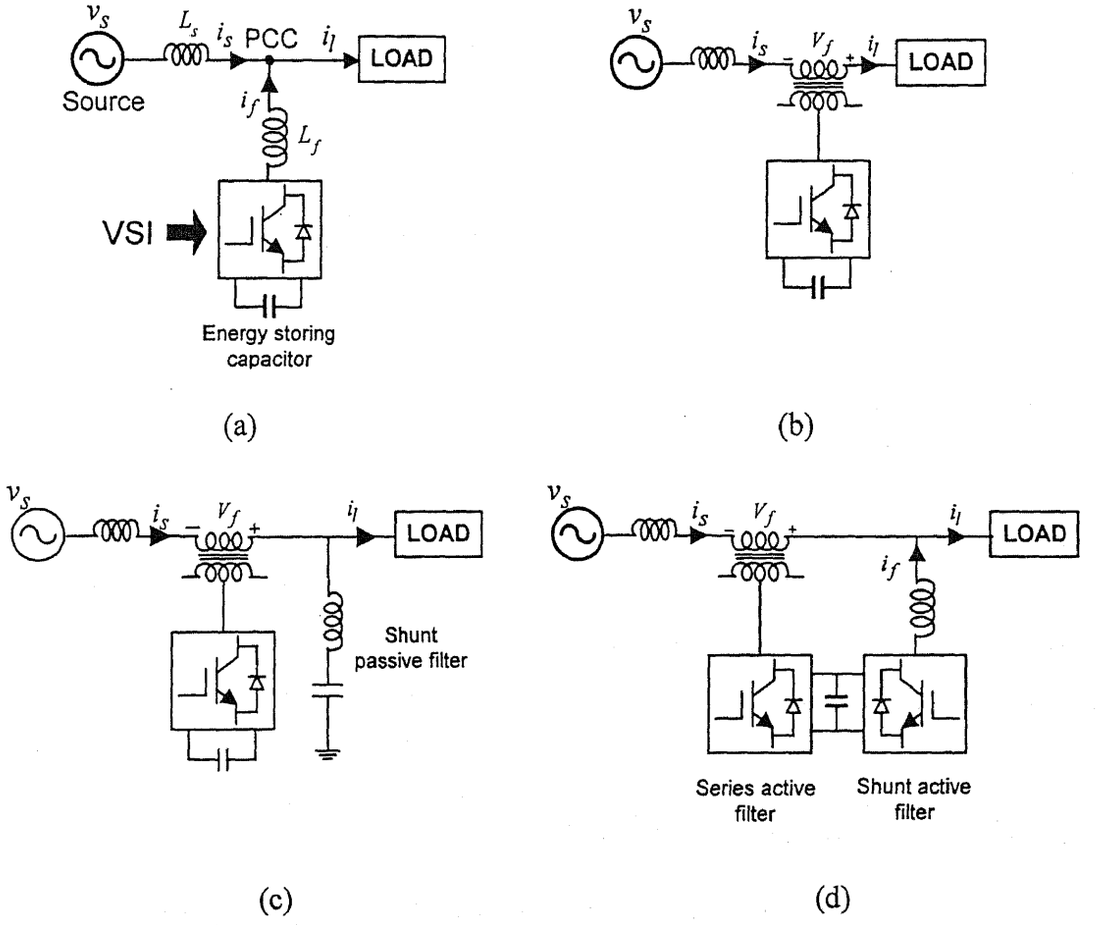


Fig. 1.1 (a) Shunt active power filter (b) Series active power filter (c) Series active and shunt passive power filter (d) Unified power quality conditioner

Series active power filter

The series active power filter shown in Fig. 1.1 (b) is connected before the load in series with the mains using a matching transformer. Its aim is to eliminate the voltage harmonics and to balance and regulate the terminal voltage of the load. Its installation helps to damp out the harmonics propagation caused by resonance with the line impedance and other

passive shunt compensators. In addition, this configuration can also be used as a Dynamic Voltage Restorer [21-24].

Hybrid Power Filters

There are many configurations of hybrid power filters [25-31]. The series active and shunt passive configuration is shown in Fig. 1.1 (c). The major advantage of this filter is that the compensation effect is no longer influenced by the impedance of the supply system. The possibility of parallel resonance between the source impedance and shunt passive LC filter vanishes because of series active filter. The required rating of the series active filter is considerably smaller than that of simple shunt active filter. Thus, hybrid filters combine the advantage of both passive and active filters without any of their disadvantages. The hybrid power filters have capability of reducing the voltage and current harmonics at a reasonable cost.

Unified Power Quality Conditioner

Unified power quality conditioner is a combination of active shunt and active series filter [32-36]. One common dc storage capacitor is shared between the active series and active shunt compensator as shown in Fig. 1.1 (d). It can be used in single and three phase configurations. It is a universal power filter, which eliminates voltage and current harmonics. However, it is expensive and its control is rather complex because of large number of switching devices involved.

1.2.3 Classification Based on Supply Systems

The active filters may also be classified depending on the supply configurations. The supply systems may be single-phase two-wire, three-phase three-wire and three-phase four-wire. There are many nonlinear loads such as domestic appliances connected to single phase supply systems. Some three-phase nonlinear loads are without neutral such as adjustable speed drives fed from three-wire supply system. Also, there are many nonlinear single-phase loads distributed on three-phase four-wire supply systems, such as computers and commercial lighting. The two wire supply systems can also be compensated using active shunt, active series, and hybrid filters and UPQCs. Compensator structure may also

be classified depending upon load connection i.e. three-phase star connected load, delta connected load [37].

In three-phase, three-wire supply system the load may be either star connected or delta connected. In fact three-phase, three-wire supply system is a special care of three-phase, four-wire supply systems, in which the neutral connecting the supply and the load, is disconnected. We shall therefore concentrate only on three-phase, four-wire systems, as it is the most general case.

To realize the active shunt power filters, various compensator topologies are used. For instance in [37] a single dc storage capacitor and three single-phase inverters with isolation transformers are used to realize the active shunt power filter. However, when the load current contains dc component, it does not compensate the dc component due to the presence of transformers. Neutral clamped inverter topology [38] is also well suited for ac load compensation but is not suitable to compensate loads containing ac and dc components. This is because the dc component causes voltage imbalance in capacitors. Three-phase, four-leg inverter with single dc storage capacitor topology [39] can be used for ac and dc load compensation, but it passes inverter-switching components to the system neutral.

A neutral clamped topology of an active power filter is shown in Fig. 1.2. This topology is suitable both for three-phase, three-wire and three-phase, four-wire systems. Let us assume that the load is unbalanced. Then there will be a neutral current in case the point n is connected to either n' or N or both. There are three possible neutral connections. These are discussed below.

- In a three-phase, four-wire distribution system, points N and n are connected by the neutral conductor. The sum of load currents will be non-zero when any unbalance is present in the load. In this case the zero sequence load current can be made to circulate between the compensator and the load if the path $n-n'$ is present. The supply neutral will then be free of the zero sequence current.
- In a three-phase, three-wire distribution system, the connection $N-n$ is absent. In this case if the path $n-n'$ is present, the zero sequence current will again circulate in this path.

- In a three-phase, three-wire distribution systems, if the neutral path $n-n'$ is also absent, there will not be any zero sequence current at any point of the network. However the voltages between $N-n'$ and $n-n'$ will now oscillate.

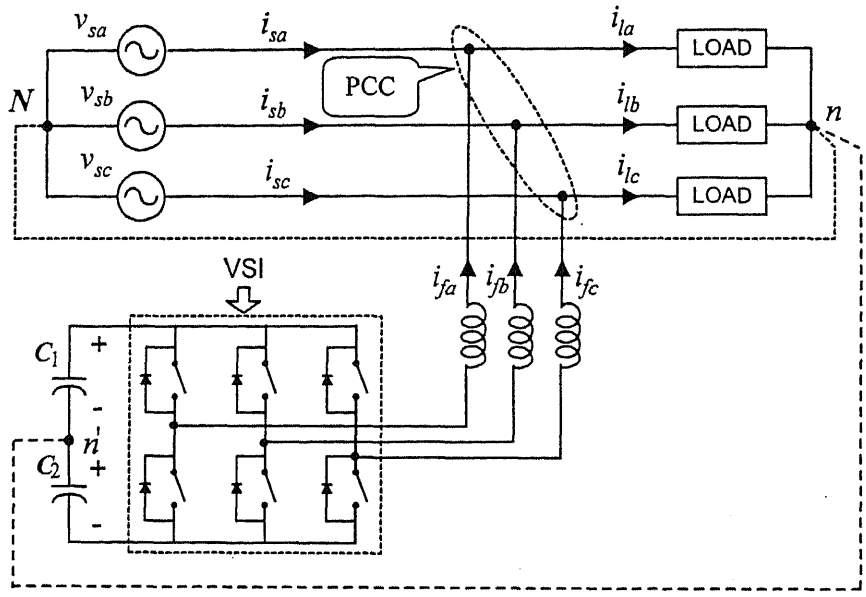


Fig. 1.2 Active power filter for three-phase supply systems

1.2.4 DSTATCOM Operating Modes

In this thesis, a shunt active power filter topology for three-phase, four-wire distribution system is chosen for detailed investigation. The filter is connected in parallel with the load being compensated as shown in Fig. 1.2. The VSI is generally operated in the current control mode. In the following discussion, this topology will be referred by the name Distribution Static Compensator (DSTATCOM) or simply compensator or filter. The DSTATCOM thus consists of an inverter circuit, dc storage capacitors and interface inductors. The dc side of the DSTATCOM is connected to energy storage capacitor(s) and the ac side is connected to the ac bus through a filter inductor (also called interface inductor). The point at which the compensator is connected in parallel to the load is called Point of Common Coupling and is denoted by PCC. The ac bus can supply various loads including non-linear ones. The compensator is controlled in a closed loop i.e. the inverter switches are controlled to follow the current control command. Interface inductor helps to convert the voltage output created by the inverter to a current output. The voltage across the interface inductance determines the maximum di/dt that can be achieved by the

compensator. This is important in the sense that relatively high values of di/dt may be needed to cancel higher order harmonic components. Therefore the choice of interface inductor is crucial. For instance, a large interface inductor may be better for isolation from distribution system and protection from transient disturbances. However, large inductor would limit the ability of the compensator to cancel higher order harmonics. The bandwidth of the inverter will also depend upon the level of voltage of dc capacitors and hysteresis band of the control.

In ideal situation, the compensator is required to supply the reactive power of the load and therefore the dc capacitor voltage should remain constant. In practice however, there are losses in the inverter and interface inductor. These losses are to be supplied from the source to hold the capacitor voltage to a constant value. This is important from the compensator performance point of view.

The DSTATCOM can be operated in two modes i.e. DSTATCOM in current control mode and DSTATCOM in voltage control mode.

DSTATCOM in Current Control Mode

In the current controlled mode, the compensator injects the currents (i_f) at point of common coupling (PCC) in such a way that the harmonic components and unbalances in the load currents are nullified. The single line diagram of DSTATCOM in current control mode is shown in Fig. 1.3. This topology is most commonly used for power factor correction, load balancing and harmonic elimination.

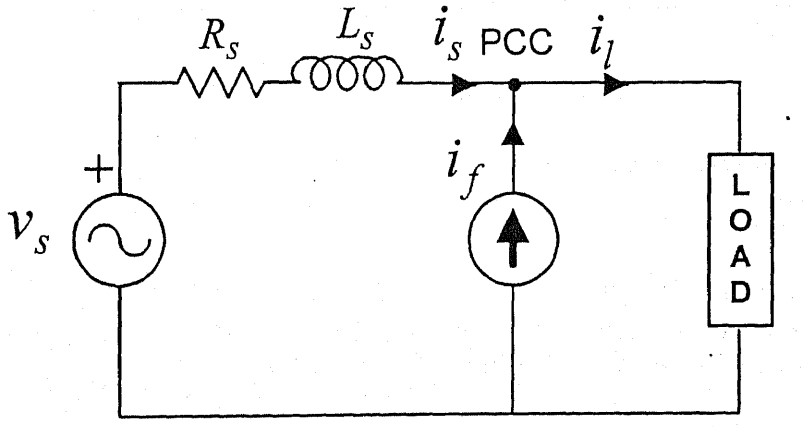


Fig. 1.3 DSTATCOM in current control mode

DSTATCOM in Voltage Control Mode

In the voltage controlled mode, the compensator maintains the nominal balanced and sinusoidal voltage at the point of common coupling. This DSTATCOM mode is employed where the PCC voltage is distorted and unbalanced which may be objectionable to other sensitive loads connected to the bus. The single line diagram of DSATACOM in voltage control mode is shown in Fig. 1.4. The objective here is to protect the sensitive loads from an upstream poor quality supply.

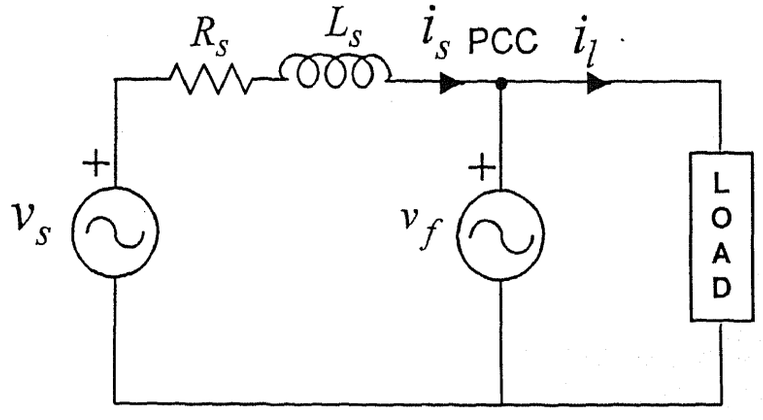


Fig. 1.4 DSTATCOM in voltage control mode

1.3 CONTROL ASPECTS OF SHUNT ACTIVE FILTERS

The following issues are involved in the control of the shunt active power filters:

- Measurements of voltage and current signals.
- Extraction of reference quantities (Reference compensator currents, reference filter capacitor voltage, etc.).
- Control of dc capacitor voltages.
- Generation of switching control commands for semiconductor switches.

The voltage and current transducers are used for measurement of voltage and current transducers at various points in the system circuit. These provide isolated low-level signals, which are fed to PC through ADC card for use in control algorithm.

For DSTATCOM in current control mode, generation of reference compensator currents is an important issue. Reference currents are computed using suitable control algorithm taking samples of load currents and PCC terminal voltages. The actual compensator currents must follow or track the reference currents that are function of the load currents. However the load current is not known a priori. Further, the load current may change at any instant. Therefore on-line computation of reference current is a critical issue in the design of the active power filters.

Various methods have been proposed for generating reference compensator current in literature [40-52]. The sampling and averaging techniques of load compensation were proposed by L. Gyugyi [40-42]. These methods of load compensation are able to supply only the fundamental reactive power of the load. However these methods do not work for a time varying and/or non-linear load. Out of many methods for generating the compensator reference currents, the *pq* theory [43-44] has gained considerable attention and is well established.

The compensation scheme based on the *pq* theory can eliminate all unbalances and harmonics caused by non-linear time varying load provided source voltages are balanced and sinusoidal and power converter has sufficient bandwidth to track the reference compensator currents. However when the source voltages are unbalanced the scheme does not provide satisfactory results. Furthermore, generation of reference currents is computation intensive due to $\alpha\beta 0$ and inverse $\alpha\beta 0$ transformation. On the other hand, load compensation based on instantaneous theory of symmetrical components [37, 45-46] is much simpler than *pq* theory. It does not require complex transformations of currents.

Generalized instantaneous reactive power theory is much more general. In this, instantaneous compensator current includes both the active and reactive power compensation. Nevertheless formulating reference current vector in terms of compensator powers does not guarantee desired source currents [47-48]. Furthermore, the formulation in [48] does not allow explicit setting of power factor of the source.

The compensator structures use one or more than one dc capacitor as an energy source to voltage source inverter. It is important that the voltage of each capacitor should be regulated to a reference voltage. This reference voltage for dc capacitors is chosen well above the peak of the ac system voltage for good performance of the compensator. In topologies where, more than one capacitors are used, there may be problem of voltage imbalance in the capacitors due to various reasons [53-57]. One of the major reasons for this voltage imbalance is the presence of a dc component in the load current [58-60]. Under this condition, if we use neutral clamped inverter topology for load compensation, one-capacitor charges and the other discharges. This leads to loss of tracking in the regions where, capacitor voltage is nearly equal or below the peak of ac system voltage. While a PI regulator holds total capacitor voltage to a constant value, an additional circuit should be used to regulate each dc capacitor voltage to a constant value.

The power switches are controlled through a driver card, which use optical isolation between high voltage power circuit and low voltage control circuit. The optical isolators are supplied from isolated power supplies.

1.4 LOAD COMPENSATION WITH UNBALANCED STIFF SOURCE

Usually in power system operation, balanced three-phase voltage in transmission systems is assumed. However, unbalanced currents resulting from unbalanced loads are usually encountered in distribution systems. In distribution systems, power is usually distributed through radial feeders. Thus an unbalance current results in unbalance three-phase voltages at the various buses. The unbalance becomes more significant in distribution systems for a feeder supplying high density demand. The shunt algorithms, i.e. *pq* theory and theory of instantaneous symmetrical components [43-44, 37, 45-46] which are used to extract reference compensator currents, provide effective operation and good performance under balanced source voltage. However when the voltage source is unbalanced, the direct application of these shunt algorithms will give large errors in compensation. Synchronous detection method [61] may be used to provide compensation under unbalanced voltages. However this method is limited to unity power factor and magnitude unbalance only.

Similar strategies have also been reported in [55] that uses complex $\alpha\beta0$ and inverse $\alpha\beta0$ transformations.

The generalized instantaneous reactive power theory [47] however does not assume balanced source voltages, but it can be easily seen that direct application of shunt algorithm will result in distorted source currents in an unbalanced source voltage. Thus the need of a simple and effective shunt algorithm is felt under these circumstances.

The poor performance of shunt algorithm under unbalanced source voltage can be understood as follows. Only three-phase balanced voltages and currents can supply constant active and reactive powers. If voltages are balanced, we can always find a set of balanced currents to supply constant real power. However if voltages are unbalanced, we can still find source currents to satisfy this power constraints (constant powers), but source currents will not remain balanced and sinusoidal.

1.5 LOAD COMPENSATION WITH A NON-STIFF SOURCE

Most of the shunt algorithms [43-46] assume the PCC voltage to be stiff. However this is not generally the case. The distribution loads are supplied through feeders. In general, there may be various feeder segments and load buses before the PCC. Thus at best the source and feeder impedance are the Thevenin equivalent obtained by looking into the network at PCC. Thus not only the feeder impedance is not known a priori, it may change suddenly depending on the loads that are connected to the upstream buses.

In such situations, the switching frequency harmonic components generated by the inverter distort both the voltages at the PCC and the source currents. The compensation algorithms generally require the measurements of local variables, i.e. the PCC voltages. Thus if the voltages are distorted due to switching frequency harmonics, the reference currents generated by the compensation algorithm will also be distorted. Thus a straightforward application of compensation algorithm can result in poor compensation.

To pass the inverter switching frequency components a filter capacitor may be connected in parallel with the compensator at PCC. However, the presence of the capacitor causes problem as it changes the dynamics of the compensating system. A hysteresis based

current controller can not be used now for this purpose. A more robust and effective control algorithm is required to provide correct compensation schemes with non-stiff source.

It is sometimes desired that the upstream or PCC voltages should be regulated to nominal value irrespective of the source voltage and load current conditions. The DSTATCOM employed in this mode is known as DSTATCOM in voltage control mode.

1.6 OBJECTIVES OF THE THESIS

Keeping in view of the above considerations we define the following objectives of the thesis.

1. To evolve a general algorithm for various kinds of shunt compensation schemes.
2. To find a suitable topology which works for compensation of load currents with ac and dc components under balanced and unbalanced voltages.
3. To provide a control algorithm for load compensation when the source is not stiff.
4. To provide DSTATCOM control to regulate the bus voltage at the nominal value.

Research has been carried out to achieve the above mentioned objectives and the major contributions of the thesis are:

1. A shunt algorithm is proposed based on generalized instantaneous reactive power theory [47]. This is called the generalized theory as all other theories e.g. *pq* theory [43-44], theory of instantaneous symmetrical components [37, 45-46] can be derived from it. By appropriate selection of source power terms, we can obtain different kinds of compensation [62-63]. The general algorithm is then modified for load compensation in unbalanced source voltages. The feasibility of shunt algorithm is demonstrated by realizing DSTATCOM using neutral clamped inverter. Its performance is studied both in steady state and transient conditions. It is shown that the compensator exhibits the fast dynamic performance.
2. It is illustrated that when the load currents contain dc components in addition to ac components, the two dc capacitors in neutral clamped inverter circuit exhibit the voltage imbalance problem. The voltage imbalance in dc capacitors results in

erroneous compensation. To overcome this problem a new DSTATCOM topology is proposed [58] in which an additional chopper circuit is connected to the neutral point of the capacitors. Various control schemes of chopper are proposed to regulate the dc capacitor voltages around a reference value. This ensures the correct performance of the compensator for load currents containing dc components.

3. To overcome the voltage distortion problem when the source voltage is not stiff, fundamental of the PCC voltages is extracted and fed to the shunt algorithm. In addition, a state feedback hysteresis band controller is used for tracking the control signal. An interesting feature of this control is that the inverter switching frequency components are highly attenuated in the source current and the PCC voltage. It is demonstrated that for balanced and sinusoidal upstream source voltage, the proposed control gives excellent performance. The control scheme also produces satisfactory performance when the upstream source voltage is distorted.

4. An algorithm to operate DSTATCOM in voltage control mode is suggested which regulates the bus voltage at a nominal value. A dead-beat control for switching of the inverter is used. The DSTATCOM in this mode is able to maintain nominal balanced and sinusoidal voltages irrespective of distortion either on the source or the load side.

1.7 OUTLINE OF THE THESIS

Chapter 1 introduces the concept of load compensation and voltage regulation using DSTATCOM. A detailed literature review is also presented.

Chapter 2 begins with the discussion on general theory of shunt compensation. Various shunt compensation theories, i.e., sampling and averaging techniques, source current synthesis using capacitor voltage feedback, *pq* theory, load compensation using instantaneous symmetrical component theory and generalized instantaneous reactive power theory are described. Based on the generalized instantaneous reactive power theory, a shunt algorithm is proposed for various kinds of compensation schemes. The general algorithm is then modified to tackle unbalanced source voltages. All the above algorithms are verified through detailed simulation and experimentation with an ideal inverter.

In **Chapter 3**, various DSTATCOM topologies are described to realize shunt compensator for ac load compensation. Neutral clamped inverter topology is chosen for ac load compensation in the three-phase, four-wire distribution systems. The control loop for dc capacitors voltage is described. The state space model of the compensator is developed. The voltage source inverter is operated in a hysteresis band current control mode. Based on the state space model, the simulation results for the steady state and the transient performance of the compensator are presented. The balanced as well as unbalanced source voltages are considered. The simulation results are also verified through experimental results.

A new DSTATCOM topology called neutral clamped inverter-chopper topology is proposed for compensation of loads with ac and dc components in **Chapter 4**. It is compared with other existing topologies. Due to the presence of a dc component in the load current, the dc capacitors face voltage imbalance problem i.e., one capacitor discharges while the other charges. To solve this imbalance problem, a chopper circuit in addition to the neutral clamped inverter circuit, is used. Various chopper control schemes are presented and they are verified through simulation. Some selected schemes are also verified through experiments.

In **Chapter 5**, load compensation with non-stiff source is considered. It is demonstrated that if we apply shunt algorithm for stiff voltage source to a system with non-stiff voltage source, it results in distorted PCC voltage. To eliminate these distortions a fundamental extraction algorithm is used and a state feedback switching controller is designed. This guarantees that the PCC voltage as well as source currents are perfectly balanced and sinusoidal. Thus in addition to the load compensation the compensator also regulates the terminal voltage. However, source currents may not remain balanced and sinusoidal when upstream source voltages are unbalanced and contain harmonics. All the above points are demonstrated through digital simulation and experimental results.

DSTATCOM that operates in voltage control mode to regulate the voltage of PCC is designed in **Chapter 6**. The magnitude of the PCC voltage can be arbitrarily chosen while its phase angle is obtained by the dc capacitor voltage control loop. This control loop

ensures that the source supplies the active power to the load and losses in the inverter. It is demonstrated that under unbalanced source voltage and load currents, the PCC voltage is regulated at the nominal value. Detailed simulation and experimental results are also presented.

The thesis ends in **Chapter 7** where, the general conclusions derived from the thesis are presented and some scope for future work is suggested.

The experimental set up used in the laboratory is given in Appendices.

CHAPTER 2

GENERAL THEORY OF SHUNT COMPENSATION

Originally, passive filters were evolved for high voltage dc transmission systems in order to reduce the harmonic voltages and currents in the ac power network to acceptable levels. Later on these were also used for balancing an unbalanced load. However the passive filters have certain disadvantages, which are overcome by active power devices (filters). The active power filters have been proposed by eminent researchers in 1970's [4-6]. Recent progress in voltage and current rating and switching speed of semiconductor devices such as IGBTs, GTO thyristors, has spurred interest in the study of active power filters with the focus on practical applications. The sophisticated PWM inverter technology along with the recently developed control methods [43-52] has made it possible to put active power filters into commercial installations. In the last couple of decades, the researchers have evolved many efficient theories of shunt compensation to control the active shunt devices. The main purpose of the shunt active power compensator is to cancel the effects of poor load power factor, harmonic currents and unbalance in the load. The dc components in the load current can also be cancelled by choosing a suitable compensator configuration. As a result of this compensation, source currents are balanced and sinusoidal.

In this chapter we shall discuss the various theories of shunt compensation starting from sampling and averaging techniques proposed in 1970's [40-41], to the most recent ones, i.e., instantaneous reactive power theory [43-44], generalized reactive power theory [47-48], and theory of instantaneous symmetrical components [37, 45-46].

Further in this chapter, a new generalized algorithm for shunt compensators is proposed. These various compensators have been demonstrated through digital simulation. The feasibility of the proposed algorithm has been verified through experiments. The algorithm has also been modified and applied in situations where the system voltages are unbalanced.

To illustrate the functioning of a shunt compensator, consider the three-phase, four-wire distribution system shown in Fig. 2.1. All the currents and voltages that are indicated in this figure are instantaneous quantities. Here a three-phase balanced supply (v_{sa}, v_{sb}, v_{sc}) is connected across a star (Y) connected load. The loads are such that the load currents (i_{la}, i_{lb}, i_{lc}) may not be balanced, may contain harmonics and dc offset. In addition, the power factor of the load may be poor. One implication of the load not being balanced in this system is that, there may be zero-sequence current i_o flowing in the neutral wire $n-N$.

The shunt compensator is represented by three ideal current sources i_{fa}, i_{fb} and i_{fc}. The shunt compensator is connected to the system at the point of common coupling (PCC). The current sources are connected in star with their neutral n' being connected to the neutral wire. The purpose of the shunt compensator is to inject currents in such a way that the source currents (i_{sa}, i_{sb}, i_{sc}) are harmonic free balanced sinusoids and their phase angle with respect to the source voltages (v_{sa}, v_{sb}, v_{sc}) has a desired value. The zero sequence current i_o is limited to path $n-n'$ thereby preventing current flow in $N-n'$.

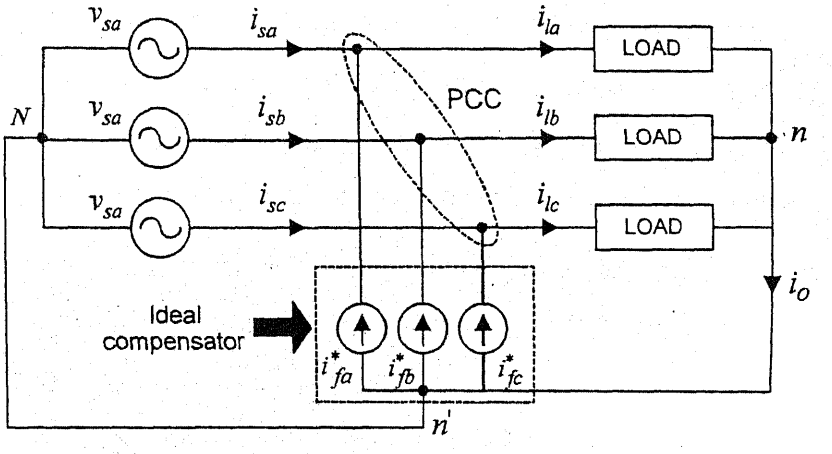
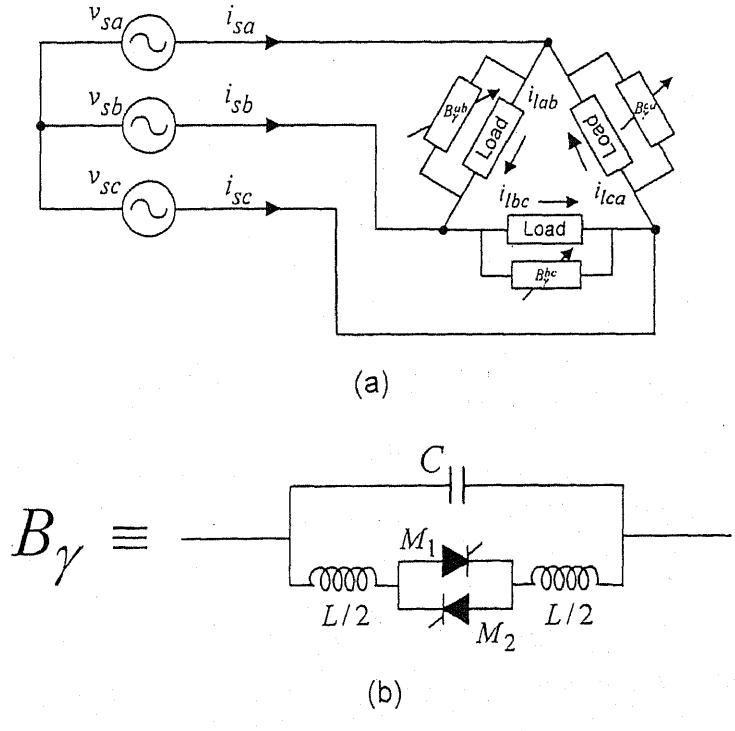


Fig. 2.1 Schematic diagram of a shunt compensator for three-phase, four-wire distribution system

In the following sections the various techniques and theories of load compensation using shunt devices (shunt active power filters) will be discussed.

2.1 SAMPLING AND AVERAGING TECHNIQUES

The problem of balancing the unbalanced delta connected load was originally investigated by C. P. Steinmetz at the beginning of this century. Steinmetz showed that "Any unbalanced linear ungrounded three-phase load can be transformed into a balanced, real three-phase load without changing the real power exchange between source and load, by connecting an ideal, purely reactive compensating network in parallel with it" [42]. However, with time varying loads, the realization of compensating network with reactive elements (capacitor and inductors) was not feasible. Later on, with the advent of semiconductor power devices the realization of time varying reactive network became a reality. In 1978, L. Gyugyi proposed sampling and averaging techniques to realize thyristor controlled time varying reactive network [40-41]. These methods are discussed in detail in [42]. To illustrate the basic idea, we consider three-phase system, delta connected load as shown in Fig. 2.2 (a).



(a)

(b)

Fig. 2.2 Load compensation using sampling and averaging technique (a) Compensated system (b) Dynamic susceptance for compensation

The compensator circuit that generates susceptance B_γ for each phase is shown in Fig. 2.2 (b). By changing the firing angle of the thyristors we change the effective reactance of the compensator and hence obtain the desired compensation. The dynamic susceptance (B_γ) is computed such that it is able to cancel only reactive power at fundamental frequency. The algorithm for dynamic susceptance for compensation of load shown in Fig. 2.2 (a) is as follows [40-41].

$$\left.\begin{aligned} B_\gamma^{ab} &= \frac{1}{3\sqrt{3}V^2}\frac{1}{T}\int_0^T (v_{bc}\,i_{sa} + v_{ca}\,i_{sb} - v_{ab}\,i_{sc})\,dt \\ B_\gamma^{bc} &= \frac{1}{3\sqrt{3}V^2}\frac{1}{T}\int_0^T (-v_{bc}\,i_{sa} + v_{ca}\,i_{sb} + v_{ab}\,i_{sc})\,dt \\ B_\gamma^{ca} &= \frac{1}{3\sqrt{3}V^2}\frac{1}{T}\int_0^T (v_{bc}\,i_{sa} - v_{ca}\,i_{sb} + v_{ab}\,i_{sc})\,dt \end{aligned}\right\} \qquad (2.1)$$

The above method of computation is called averaging technique. The dynamic impedance can also be computed on the basis of current samples. Using this method the algorithm for dynamic admittance is given as,

$$\left.\begin{aligned} B_\gamma^{ab} &= -\frac{1}{3\sqrt{2}V}\left[i_{sa}\Big|_{\substack{v_{sa}=0 \\ dv_{sa}\ dt>0}} + i_{sb}\Big|_{\substack{v_{sb}=0 \\ dv_{sb}\ dt>0}} - i_{sc}\Big|_{\substack{v_{sc}=0 \\ dv_{sc}\ dt>0}} \right] \\ B_\gamma^{bc} &= -\frac{1}{3\sqrt{2}V}\left[-i_{sa}\Big|_{\substack{v_{sa}=0 \\ dv_{sa}\ dt>0}} + i_{sb}\Big|_{\substack{v_{sb}=0 \\ dv_{sb}\ dt>0}} + i_{sc}\Big|_{\substack{v_{sc}=0 \\ dv_{sc}\ dt>0}} \right] \\ B_\gamma^{ca} &= -\frac{1}{3\sqrt{2}V}\left[i_{sa}\Big|_{\substack{v_{sa}=0 \\ dv_{sa}\ dt>0}} - i_{sb}\Big|_{\substack{v_{sb}=0 \\ dv_{sb}\ dt>0}} + i_{sc}\Big|_{\substack{v_{sc}=0 \\ dv_{sc}\ dt>0}} \right] \end{aligned}\right\} \qquad (2.2)$$

These techniques have been carried out only for sinusoidal steady state conditions. Thus the above can only eliminate the fundamental reactive power in steady state.

2.2 FFT TECHNIQUES

In this technique fast Fourier transform (FFT) is performed on the sample load current waveforms [64-65]. A current waveform is then synthesized that has the same harmonic components as the load currents with opposite phase angles.

However this method would require a digital signal processor (DSP) to perform FFT calculations. Basically the calculation is performed in each cycle and the desired compensation is implemented in next cycle. Therefore this clearly adds one cycle delay which could be a problem for nonlinear loads with rapidly varying characteristics. Further only a limited number of harmonics can be calculated and compensated in the available time. Therefore, FFT techniques have not been used extensively.

2.3 SOURCE CURRENT SYNTHESIS USING CAPACITOR VOLTAGE FEEDBACK

In this scheme, shown in Fig. 2.3, a VSI follows the reference currents by operating in current control mode. The reference currents are generated by a three-phase sinewave generator which is phase locked to the supply voltages [18-19, 52, 66]. The reference currents are usually in phase with the supply voltages, though the other values are possible. The magnitude of the reference sinewaves is adjusted by a feedback loop which regulates the dc capacitor voltage (v_c) to a reference value (V_{cref}). The reference value is set above the peak of supply voltages. The error is defined $e = v_{cref} - v_c$. The magnitude of sinusoidal reference source current (k) is computed using a proportional plus integral (PI) controller and it is given by

$$k = K_p\, e + K_i \int e\, dt \tag{2.3}$$

where K_p and K_i are proportional and integral gains of the PI controller. The reference source current is phase locked with the source voltage for unity power factor operation and its magnitude is taken as k from (2.3). The reference filter current is then obtained by subtracting $k \sin \omega t$ from the load current for the respective phases and this current is

tracked through the VSI. The main theme here is that if the dc capacitor voltage is maintained, then the source is supplying both the load power and the inverter losses.

One may also employ PD controller at medium or low level voltage of distribution systems. In [52, 66], it is claimed that a PD controller is the most natural choice. The advantage with the PD controller is that the dc capacitor charge reduces a bit from its set reference value, because there is always a constant steady state error. The PD controller also stops any overshoot or sharp fall in the dc capacitor voltage. In PI controller if the correction is not proper, then the voltage will rise or fall monotonically.

The main drawback of the scheme is that it has a very slow response due to the absence of any direct control on the power flow. The other disadvantage is that if by any chance the value of k becomes negative, the inverter will supply both the source and the load. This will increase the rating of the inverter and has the potential for damaging the inverter.

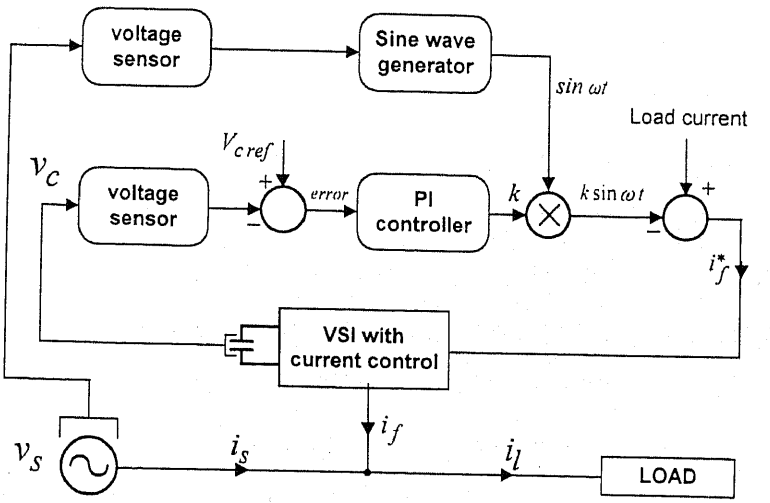


Fig. 2.3 Source current synthesis using capacitor voltage feedback

2.4 INSTANTANEOUS PQ THEORY

The *pq* theory was proposed by H. Akagi, Y. Kanazawa and A. Nabae in 1983 [43-44]. It is also called instantaneous reactive power theory. Before *pq* theory various methods of load compensation were proposed using static converters [6, 40-41]. However these methods can eliminate only the fundamental reactive power in steady state as discussed in Section 2.1. The *pq* theory on the other hand, not only compensates the fundamental reactive power

under transient conditions but also compensates for harmonic currents in the load. Ideally, the compensation based on *pq* theory can eliminate all unbalances and harmonics caused by non-linear, time varying load currents (i_{la}, i_{lb}, i_{lc}), shown in Fig. 2.1, provided source voltages (v_{sa}, v_{sb} and v_{sc}) are balanced sinusoids and the power converter has infinite bandwidth to track the reference filter currents (i_{fa}, i_{fb}, i_{fc}). The *pq* theory uses $\alpha-\beta-0$ transformation and various definitions of active and reactive powers. These are described in the following.

Using $\alpha-\beta-0$ transformation on the instantaneous voltages and currents v_a, v_b, v_c and currents i_a, i_b, i_c, we have

$$\begin{bmatrix} v_o \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.4}$$

$$\begin{bmatrix} i_o \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.5}$$

Let the instantaneous real, imaginary and zero sequence powers be denoted by p, q and p_o respectively. Then the three phase instantaneous power is given by

$$p_{3\phi} = v_a i_a + v_b i_b + v_c i_c \tag{2.6}$$

Then using inverse of transformations in (2.4)-(2.5), we get

$$\left.\begin{aligned} p_{3\phi} &= v_\alpha i_\alpha + v_\beta i_\beta + v_o i_o \\ &\equiv p + p_o \end{aligned}\right\} \tag{2.7}$$

The instantaneous reactive power, q is defined as

$$q = v_\alpha i_\beta - v_\beta i_\alpha = \frac{1}{\sqrt{3}}\{i_a(v_c - v_b) + i_b(v_a - v_c) + i_c(v_b - v_a)\} \tag{2.8}$$

It represents an energy that may or may not be constant and it is being exchanged between the phases of the system. This implies that q does not contribute to the energy transfer between the source and the load at any time. This is illustrated in Fig. 2.4 (a). From (2.7)-(2.8), we write p and q as follows.

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.9}$$

This gives the following expression for currents.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \tag{2.10}$$

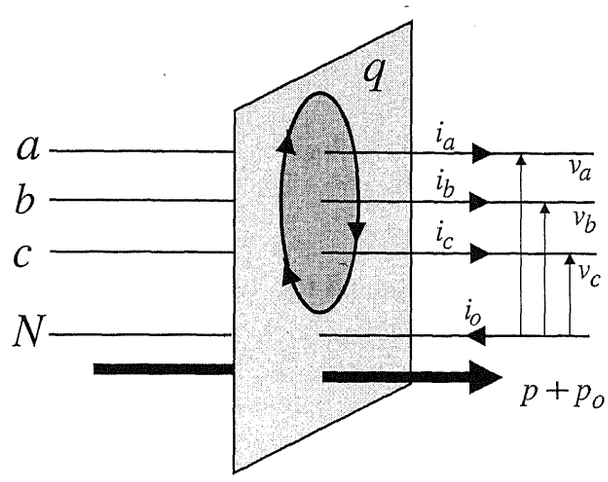
where $i_{\alpha p}$, $i_{\alpha q}$ and $i_{\beta p}$, $i_{\beta q}$ are components of currents i_α and i_β respectively. From (2.10), we define

$i_{\alpha p} = \dfrac{v_\alpha}{v_\alpha^2 + v_\beta^2} p$ is the α-axis instantaneous active current

$i_{\alpha q} = -\dfrac{v_\beta}{v_\alpha^2 + v_\beta^2} q$ is the α-axis instantaneous reactive current

$i_{\beta p} = \dfrac{v_\beta}{v_\alpha^2 + v_\beta^2} p$ is the β-axis instantaneous active current

and $i_{\beta q} = \dfrac{v_\alpha}{v_\alpha^2 + v_\beta^2} q$ is the β-axis instantaneous reactive current.



q : circulating energy between phases
$p+p_o$: instantanous active 3 – phase active power

Fig. 2.4 (a) Power flow related to *a-b-c* reference frame

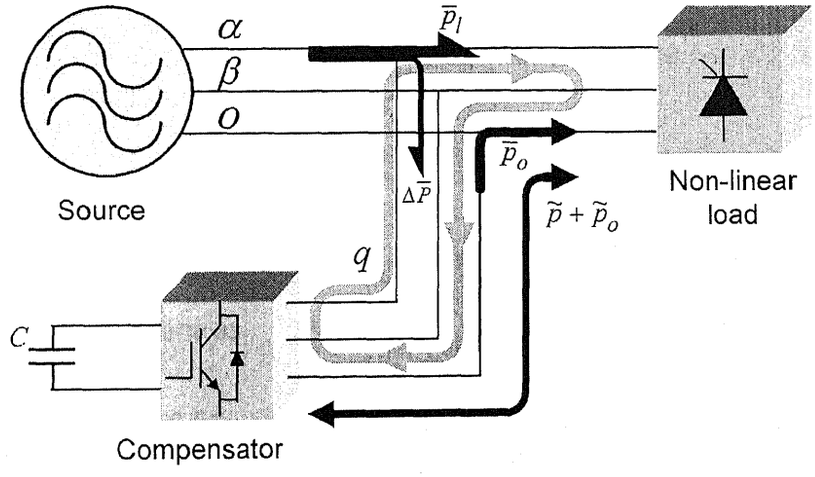


Fig. 2.4 (b) Power flow related to $\alpha-\beta-0$ reference frame

The real instantaneous power p can be divided into components p_α and p_β. Substituting the definitions of current components in (2.9), it can be shown that

$$p = p_\alpha + p_\beta \tag{2.1}$$

where.

$$\left.\begin{aligned} p_\alpha &= v_\alpha\, i_{\alpha p} = \frac{v_\alpha^2}{v_\alpha^2 + v_\beta^2}\, p \\ p_\beta &= v_\beta\, i_{\beta p} = \frac{v_\beta^2}{v_\alpha^2 + v_\beta^2}\, p \end{aligned}\right\} \tag{2.12}$$

Similarly, the reactive power q can be divided into two components corresponding to the products of voltage along α axis and current along β axis and vice versa.

$$q = -v_\beta\, i_{\alpha q} + v_\alpha\, i_{\beta q} \tag{2.13}$$

From (2.7) and (2.11), the instantaneous three-active phase power is given by

$$p_{3\phi} = p_\alpha + p_\beta + p_o \tag{2.14}$$

The instantaneous active and reactive power has two parts – a dc or average value indicated by overbar (–) and an alternating component indicated by overtilde (~). Thus we can write,

$$p = \bar{p} + \tilde{p} \tag{2.15}$$

$$q = \bar{q} + \tilde{q} \tag{2.16}$$

$$p_o = \bar{p}_o + \tilde{p}_o \tag{2.17}$$

The load powers that can be compensated in terms of $\alpha - \beta - 0$ axis are $\tilde{p}_l$, $\bar{q}_l$, $\tilde{q}_l$ and $p_o = \bar{p}_o + \tilde{p}_o$. The compensator needs an energy storage element, usually a dc capacitor to supply the zero mean oscillating powers $\tilde{p}_l$ and $\tilde{q}_l$ and $\tilde{p}_o$. The average reactive power $\bar{q}_l$ can be supplied by the compensator fully or partially. The average zero sequence power $\bar{p}_o$ can not be directly supplied from the compensator as it is a real power unless capacitor is supplied by a battery. A more convenient approach is to draw this component of power

from the source in addition to the real power $\bar{p}_l$. This is done with the help of a feedback loop which regulates the dc capacitor voltage to a reference value. The average power loss in the inverter P_{loss} is also supplied from the load by the same approach. The above description is shown in Fig. 2.4 (b).

Let us assume that the compensator supplies a reactive power q_f, which may be equal to load reactive power. Thus,

$$q_f = q_l \tag{2.18}$$

Similarly, instantaneous active power supplied by the compensator to the load

$$p_f = \tilde{p}_l + \bar{p}_o + P_{loss} \tag{2.19}$$

The term P_{loss} refers the average real power accounting for losses in the inverter. It is obtained from the voltage regulator. Referring to compensator structure as shown in Fig. 2.1, the compensator reference currents using (2.10) are given as,

$$\begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} p_f \\ q_f \end{bmatrix} \tag{2.20}$$

Substituting filter powers q_f and p_f from (2.18) and (2.19), we get reference filter currents in $\alpha - \beta - 0$ frame as

$$\begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} \tilde{p}_l + \bar{p}_o + P_{loss} \\ q_l \end{bmatrix} \tag{2.21}$$

Finally, through $\alpha - \beta - 0$ inverse transformation we compute the filter reference currents in $a - b - c$ phase system

$$\begin{bmatrix} i^*_{fa} \\ i^*_{fb} \\ i^*_{fc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_o \\ i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} \tag{2.22}$$

where i_o is the zero sequence currents of the load current (2.5) and is given by

$$i_{lo} = \frac{1}{\sqrt{3}}(i_{la} + i_{lb} + i_{lc}) \tag{2.23}$$

The over all block diagram of the compensated system is shown in Fig. 2.5.

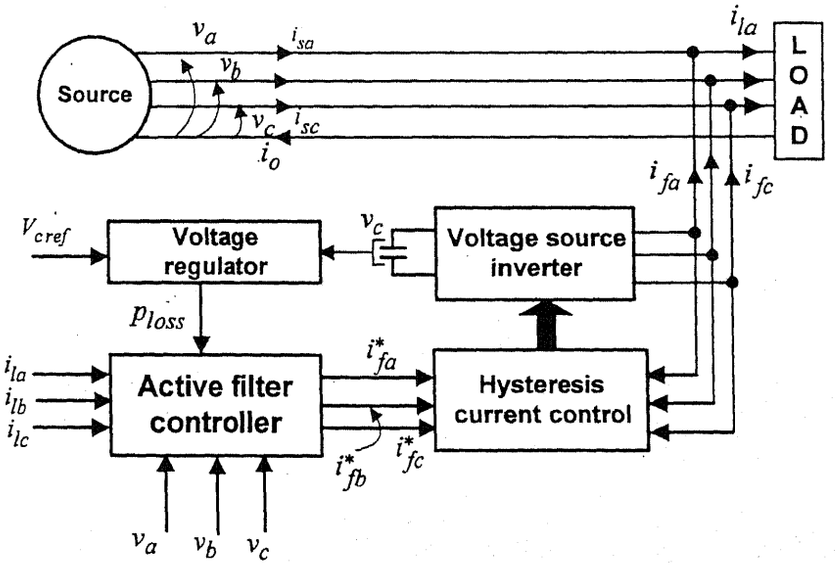


Fig. 2.5 Block diagram of shunt active power filter in 3-phase, 4-wire distribution system

The *pq* theory, though an elegant and revolutionary step in the field of load compensation however has the following limitations.

- If the source voltages are unbalanced and non-sinusoidal, the *pq* theory fails.
- It needs a large number of transducers of measurement and intensive computation including complex transformations, which makes the system operation complex.

2.5 THEORY OF INSTANTANEOUS SYMMETRICAL COMPONENTS

The theory of instantaneous symmetrical components [37, 45-46] can be used for the purpose of load balancing, harmonic suppression, and power factor correction. Algorithms provided by instantaneous symmetrical component theory can practically compensate any kind of unbalance and harmonics in the load, provided we have a high band width current source to track the filter reference currents. These algorithms have been derived in this section. For any set of three-phase instantaneous currents or voltages, the instantaneous symmetrical components are defined by [67],

$$\begin{bmatrix} i_{a0} \\ i_{a1} \\ i_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.24}$$

Similarly for three-phase instantaneous voltages, we have,

$$\begin{bmatrix} v_{a0} \\ v_{a1} \\ v_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.25}$$

In the above equations, $a = e^{j120^\circ}$. It is to be noted that the instantaneous vectors i_{a1} and i_{a2} are complex conjugate of each other and i_{a0} is a real quantity which is zero if the currents are balanced. Like *pq* theory, we assume that the supply voltages are balanced.

2.5.1 Compensating star connected load

The objective in either three or four-wire system compensation (Fig. 2.1) is to provide balanced supply current such that its zero sequence component is zero. We therefore have

$$i_{sa} + i_{sb} + i_{sc} = 0 \tag{2.26}$$

We now use (2.24)-(2.25) to compute vectors v_{sa1} and i_{sa1} from the instantaneous values of v_{sa}, v_{sb}, v_{sc} and i_{sa}, i_{sb}, i_{sc} respectively. Furthermore, the angle between the v_{sa1}

and i_{sa1} is the power factor angle between the balanced supply voltage and supply current. In the following algorithm this angle can be explicitly set to any desired value. This angle is not directly expressed in the *pq* theory described in Section 2.4.

If we now assume that the phase of the vector i_{sa1} lags that of v_{sa1} by an angle ϕ, we get

$$\angle\{v_{sa} + av_{sb} + a^2 v_{sc}\} = \angle\{i_{sa} + ai_{sb} + a^2 i_{sc}\} + \phi \tag{2.27}$$

Substituting the values of a and a^2 in the above equation can be expanded as

$$\angle\left\{\left(v_{sa} - \frac{1}{2}v_{sb} - \frac{1}{2}v_{sc}\right) - j\frac{\sqrt{3}}{2}(v_{sb} - v_{sc})\right\} = \angle\left\{\left(i_{sa} - \frac{1}{2}i_{sb} - \frac{1}{2}i_{sc}\right) - j\frac{\sqrt{3}}{2}(i_{sb} - i_{sc}) + \phi\right\}$$

Equating the angles, we can write from the above equation

$$\tan^{-1}(K_1/K_2) = \tan^{-1}(K_3/K_4) + \phi \tag{2.28}$$

where,

$$K_1 = \frac{\sqrt{3}}{2}(v_{sb} - v_{sc}),\ K_2 = v_{sa} - \frac{1}{2}v_{sb} - \frac{1}{2}v_{sc},\ K_3 = \frac{\sqrt{3}}{2}(i_{sb} - i_{sc}) \text{ and } K_4 = i_{sa} - \frac{i_{sb}}{2} - \frac{i_{sc}}{2}$$

Taking tangent to both sides of (2.28), we get

$$\frac{K_1}{K_2} = \tan\left[\tan^{-1}(K_3/K_4) + \phi\right] = \frac{K_3/K_4 + \tan\phi}{1 - (K_3/K_4)\tan\phi}$$

Substituting values of K_1 to K_4 in the above equation we get

$$(v_{sb} - v_{sc} - 3\gamma v_{sa})i_{sa} + (v_{sc} - v_{sa} - 3\gamma v_{sb})i_{sb} + (v_{sa} - v_{sb} - 3\gamma v_{sc})i_{sc} = 0 \tag{2.29}$$

where $\gamma \equiv \tan\phi/\sqrt{3}$. For unity power factor $\phi = 0$ hence $\gamma = 0$. It is interesting to note the implication of (2.29). If instantaneous active and reactive powers p, q are defined by (2.6) and (2.8) then.

$$q = -\tan\phi \; p$$

where the negative sign is due to the convention of ϕ being positive for lagging current. When the power factor angle is assumed to be zero, it implies that the instantaneous reactive power supplied by the source is zero. On the other hand, when this angle is non-zero, the source supplies a reactive power that is equal to $\sqrt{3}\gamma$ times instantaneous power.

It is well known that the instantaneous power in a balanced three-phase circuit is constant while for an unbalanced circuit it has a double frequency component in addition to the dc value. The presence of harmonics adds to the oscillating component of the instantaneous power. The objective of the compensator is to supply the oscillating component while the source supplies the average value of the load power, $\bar{p}_l$. Therefore we obtain

$$v_{sa}i_{sa} + v_{sb}i_{sb} + v_{sc}i_{sc} = \bar{p}_l \tag{2.30}$$

Since the harmonic component in the load does not require any real power, the source only supplies the real power required by the load.

From (2.26), (2.29)-(2.30), we get

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ (v_{sb} - v_{sc} - 3\gamma v_{sa}) & (v_{sc} - v_{sa} - 3\gamma v_{sb}) & (v_{sa} - v_{sb} - 3\gamma v_{sc}) \\ v_{sa} & v_{sb} & v_{sc} \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 0 \\ \bar{p}_l \end{bmatrix}$$

From Fig. (2.1), applying KCL at PCC

$$\left.\begin{aligned} i^*_{fa} &= i_{la} - i_{sa} = i_{la} - \frac{(v_{sa} - v_{so}) + \gamma\left(v_{sb} - v_{sc}\right)}{\Delta}\,\bar{p}_l \\ i^*_{fb} &= i_{lb} - i_{sb} = i_{lb} - \frac{(v_{sb} - v_{so}) + \gamma\left(v_{sc} - v_{sa}\right)}{\Delta}\,\bar{p}_l \\ i^*_{fc} &= i_{lc} - i_{sc} = i_{lc} - \frac{(v_{sc} - v_{so}) + \gamma\left(v_{sa} - v_{sb}\right)}{\Delta}\,\bar{p}_l \end{aligned}\right\} \tag{2.31}$$

where,

$v_{so} = \frac{1}{3}\sum_{j=a,b,c} v_{sj}$ and $\Delta = \sum_{j=a,b,c} v_{sj}^2 - 3v_{so}^2$. For balanced supply voltages $v_{so} = 0$, reference filter currents in (2.31) reduce to

$$\left.\begin{aligned} i^*_{fa} &= i_{la} - \frac{v_{sa} + \gamma\left(v_{sb} - v_{sc}\right)}{\Delta}\,\bar{p}_l \\ i^*_{fb} &= i_{lb} - \frac{v_{sb} + \gamma\left(v_{sc} - v_{sa}\right)}{\Delta}\,\bar{p}_l \\ i^*_{fc} &= i_{lc} - \frac{v_{sc} + \gamma\left(v_{sa} - v_{sb}\right)}{\Delta}\,\bar{p}_l \end{aligned}\right\} \tag{2.32}$$

It can be shown by simplifying (2.32) that if the load is balanced and ϕ is the same as that of the phase angle of the load current, the compensator currents become zero. Further, since $\sum_{j=a,b,c} i_{sj} = \sum_{j=a,b,c} i_{lj} - \sum_{j=a,b,c} i_{fj}$, the left side in a proper compensated system is zero. We therefore get

$$\sum_{j=a,b,c} i_{lj} = \sum_{j=a,b,c} i_{fj}$$

Then there are three possible cases. These are discussed below.

- In a three-phase, four-wire distribution system above summations will be non-zero when any unbalance is present in the load. In this case the zero sequence load current will flow between the compensator and the load in the path $n - n'$ of Fig. 2.1.

- In a three-phase, three-wire distribution systems, the connection $N-n$ is absent. In this case if the path $n-n'$ is present, the zero sequence current will again circulate in this path.

- In a three-phase, three-wire distribution systems, if the neutral path $n-n'$ is also absent, then the terms on the both sides of the above equation will be zero, i.e.,

$$\sum_{j=a,b,c} i_{lj} = \sum_{j=a,b,c} i_{fj} = 0$$

Hence there will be no zero sequence current at any point of the network. However the voltages between $N-n'$ and $n-n'$ will now oscillate.

2.5.2 Compensating Delta Connected Loads

The balancing of an unbalanced delta-connected load is a classical problem as described in Section 2.1. The theory of instantaneous symmetrical components can also be applied to this problem. The schematic diagram of the compensated system is shown in Fig. 2.6.

The compensator is connected between the phases in this scheme. The aim is to generate the three reference current waveforms for i_{fab}, i_{fbc}, i_{fca} denoted by i^*_{fab}, i^*_{fbc}, i^*_{fca} respectively, from the measurements of system voltages and load currents, such that the supply sees a balanced load. The requirements for the compensating currents in this case are same as that of the previous case with Y-connected load. Therefore the equations (2.26-2.27), and (2.30) are valid in this case also. As a result, (2.28) and (2.29) are also valid.

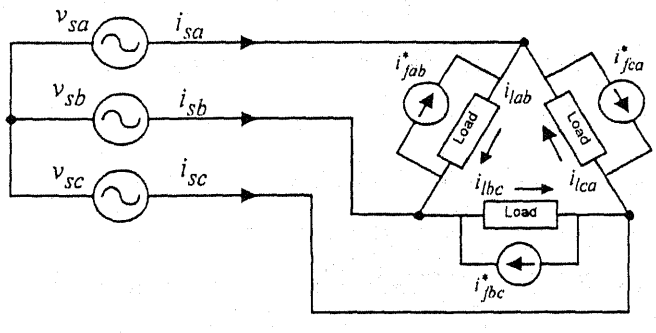


Fig. 2.6 Schematic diagram of the compensator scheme for delta-connected load

From Fig. 2.6, applying KCL at the three nodes of the delta load, we get

$$\left.\begin{aligned} i_{sa} &= i_{lab} - i^*_{fab} - i_{lca} + i^*_{fca} \\ i_{sb} &= i_{lbc} - i^*_{fbc} - i_{lab} + i^*_{fab} \\ i_{sc} &= i_{lca} - i^*_{fca} - i_{lbc} + i^*_{fbc} \end{aligned}\right\} \tag{2.33}$$

We can further write from Fig. 2.6 for zero circulating current in delta,

$$i_{lab} + i_{lbc} + i_{lca} - \left(i^*_{fab} + i^*_{fbc} + i^*_{fca}\right) = 0 \tag{2.34}$$

Substituting (2.33) in (2.29) and solving we get

$$\begin{aligned} \left(i_{lab} - i^*_{fab}\right)\left\{v_{sc} - \gamma\left(v_{sa} - v_{sb}\right)\right\} + \left(i_{lbc} - i^*_{fbc}\right)\left\{v_{sa} - \gamma\left(v_{sb} - v_{sc}\right)\right\} \\ + \left(i_{lca} - i^*_{fca}\right)\left\{v_{sb} - \gamma\left(v_{sc} - v_{sa}\right)\right\} = 0 \end{aligned} \tag{2.35}$$

Finally substituting (2.33) in (2.30) and solving, we get

$$\left(i_{lab} - i^*_{fab}\right)\left(v_{sa} - v_{sb}\right) + \left(i_{lbc} - i^*_{fbc}\right)\left(v_{sb} - v_{sc}\right) + \left(i_{lca} - i^*_{fca}\right)\left(v_{sc} - v_{sa}\right) = \bar{p}_l \tag{2.36}$$

Combining (2.34)-(2.36) we get

$$\begin{bmatrix} 1 & 1 & 1 \\ v_{sc} + \gamma\left(v_{sa} - v_{sb}\right) & v_{sa} + \gamma\left(v_{sb} - v_{sc}\right) & v_{sb} + \gamma\left(v_{sc} - v_{sa}\right) \\ \left(v_{sa} - v_{sb}\right) & \left(v_{sb} - v_{sc}\right) & \left(v_{sc} - v_{sa}\right) \end{bmatrix} \begin{bmatrix} i_{lab} - i^*_{fab} \\ i_{lbc} - i^*_{fbc} \\ i_{lca} - i^*_{fca} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \bar{p}_l \end{bmatrix} \tag{2.37}$$

From the above equation we get the reference currents as

$$\left.\begin{aligned} i^*_{fab} &= i_{lab} - \frac{v_{sab} - \gamma\left(v_{sc} - v_{so}\right)}{\Delta}\bar{p}_l \\ i^*_{fbc} &= i_{lbc} - \frac{v_{sbc} - \gamma\left(v_{sa} - v_{so}\right)}{\Delta}\bar{p}_l \\ i^*_{fca} &= i_{lca} - \frac{v_{sca} - \gamma\left(v_{sb} - v_{so}\right)}{\Delta}\bar{p}_l \end{aligned}\right\} \tag{2.38}$$

where γ, Δ and v_{so} are same as defined in Sub-section 2.5.1. In (2.38), $v_{sab} = v_{sa} - v_{sb}$ and so on. For balanced supply voltages $v_{so} = 0$.

The scheme based on instantaneous symmetrical components is computationally much simpler than *pq* theory. It does not require complex transformation of currents and voltages and many definitions of various powers [43-44, 47-48, 68-71]. Still it can transform an unbalanced non-linear load to look like a balanced adjustable power factor load on the supply side. This scheme provides a direct and comprehensive method of obtaining balanced, unity power factor source currents for all star and delta connected loads. Further it can generate the source currents at an arbitrary power factor angle. This can be beneficial from the compensator rating point of view.

2.6 GENERALIZED INSTANTANEOUS REACTIVE POWER THEORY

Akagi et al [43-44] provided elegant definition of power for compensation. However in [43-44], zero sequence components of voltages and currents are not considered. In [55, 71], zero sequence power is considered, but the formulations make the use of the orthogonal $\alpha-\beta-0$ transformation. As a consequence of this, the algorithm is computation intensive. Though, the theory of instantaneous symmetrical components for compensation [37, 45-46] is much more simplified as compared to the *pq* theory [43], however it provides less choice for different kinds of compensation.

In [47], the general definitions of reactive and active powers have been presented. In this formulation, the active and reactive powers are expressed respectively as the dot and the cross product of voltage and current vectors respectively. It is further shown that the *pq* theory is a special case of these general definitions. The instantaneous vector constructed for filter current in [47] is for a special kind of compensation where only reactive power of the load is compensated. In [48], the instantaneous compensator current vector includes both the active and reactive powers compensation. However in [48], reference compensator current vector is formulated in terms of compensator powers which makes the choice for compensator power more difficult and indirect to achieve the sinusoidal balanced source currents, particularly when a certain source power factor is desired.

In this section this theory has been applied to achieve different types of compensation schemes. Simulation results for each of these compensation schemes have been given. Experimental results have also been presented to demonstrate the feasibility of proposed general algorithm for its real time implementation.

2.6.1. Basic Definitions

The basic definitions of active and reactive powers are presented below. These are then used to define several components of currents and powers and their properties.

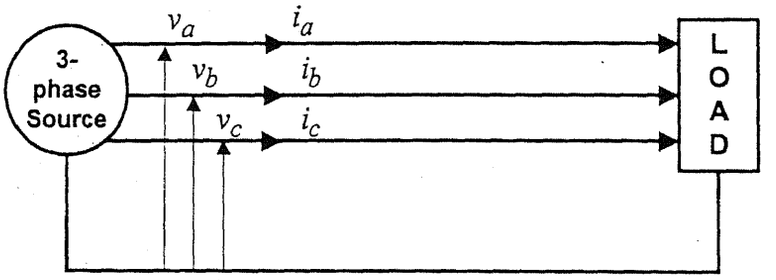


Fig. 2.7 The schematic diagram of three-phase, four-wire system

Let us consider a three-phase, four-wire system with instantaneous voltages and currents as shown in Fig. 2.7. Subscripts 'a', 'b' and 'c' denote the respective phases. The instantaneous vectors (a vector is denoted by lower case bold) are defined as

$$\boldsymbol{v} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \qquad \boldsymbol{i} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.39}$$

Fig. 2.8 shows the three-phase coordinates which are mutually orthogonal, representing phase a, phase b and phase c respectively.

The instantaneous active power is defined as the scalar (dot) product of the vectors v and i, i.e.,

$$p = \boldsymbol{v}^t \cdot \boldsymbol{i} = v_a i_a + v_b i_b + v_c i_c \tag{2.40}$$

In the above equation superscript t refers to the transpose operator. The instantaneous reactive power is a vector defined as,

$$\boldsymbol{q} = \boldsymbol{v} \times \boldsymbol{i} = \begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} = \begin{bmatrix} \begin{vmatrix} v_b & v_c \\ i_b & i_c \end{vmatrix} \\ \begin{vmatrix} v_c & v_a \\ i_c & i_a \end{vmatrix} \\ \begin{vmatrix} v_a & v_b \\ i_a & i_b \end{vmatrix} \end{bmatrix} \tag{2.41}$$

where × denotes the cross product.

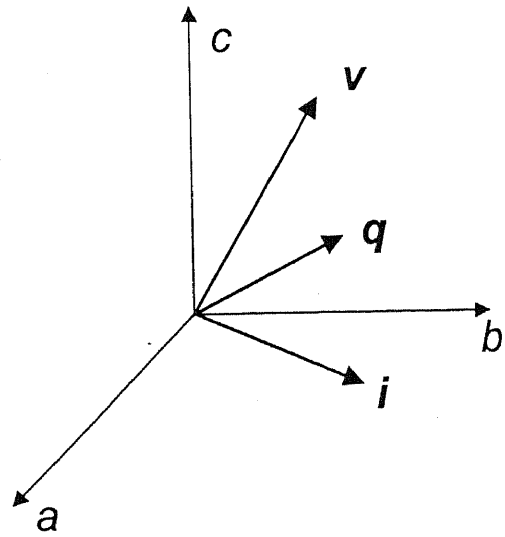


Fig. 2.8 Three-phase coordinate system

The instantaneous active current vector, $\boldsymbol{i}_p$, the instantaneous reactive current vector, $\boldsymbol{i}_q$ are defined as

$$\boldsymbol{i}_p = \begin{bmatrix} i_{ap} \\ i_{bp} \\ i_{cp} \end{bmatrix} = \frac{p}{\boldsymbol{v}^t \cdot \boldsymbol{v}} \boldsymbol{v} \tag{2.42}$$

$$\boldsymbol{i}_q = \begin{bmatrix} i_{aq} \\ i_{bq} \\ i_{cq} \end{bmatrix} = \frac{\boldsymbol{q} \times \boldsymbol{v}}{\boldsymbol{v}^t \cdot \boldsymbol{v}} \tag{2.43}$$

The instantaneous apparent power s and instantaneous power factor λ are defined as

$$s = \|\boldsymbol{v}\| \ \|\boldsymbol{i}\| \tag{2.44}$$

$$\lambda = \frac{p}{s} \tag{2.45}$$

where, $\|\boldsymbol{v}\| = \sqrt{v_a^2 + v_b^2 + v_c^2}$ and $\|\boldsymbol{i}\| = \sqrt{i_a^2 + i_b^2 + i_c^2}$ are the norms of the instantaneous voltage and current vectors respectively.

With the help of the above definitions, it is possible to establish the following properties [47-48].

- The three-phase current vector $\boldsymbol{i}$ is always equal to the sum of the instantaneous active current vector, $\boldsymbol{i}_p$ and the instantaneous reactive current vector $\boldsymbol{i}_q$, i.e.,

  $$\boldsymbol{i} \equiv \boldsymbol{i}_p + \boldsymbol{i}_q \tag{2.46}$$

- $\boldsymbol{i}_q$ is orthogonal to $\boldsymbol{v}$ and $\boldsymbol{i}_p$ is parallel to $\boldsymbol{v}$, i.e., $\boldsymbol{v}^t \cdot \boldsymbol{i}_q \equiv 0$ and $\boldsymbol{v}^t \times \boldsymbol{i}_p \equiv \boldsymbol{0}$. Thus, $\boldsymbol{i}_p$ and $\boldsymbol{i}_q$ are mutually orthogonal. Thus, $\boldsymbol{i}_p^t \cdot \boldsymbol{i}_q \equiv 0$.

- Owing to mutual orthogonality the following relations hold.

  $$i^2 = i_p^2 + i_q^2 \text{ and } s^2 = p^2 + q^2 \tag{2.47}$$

From the above discussions, it is concluded that

- The current vector $\boldsymbol{i}_p$ is indispensable for the instantaneous active power transmission, whereas $\boldsymbol{i}_q$ does not contribute to it, as $\boldsymbol{v}^t \cdot \boldsymbol{i}_q \equiv 0$ and $p = \boldsymbol{v}^t \cdot \boldsymbol{i} = \boldsymbol{v}^t \cdot \boldsymbol{i}_p$.

- The compensator needs no energy source to eliminate the instantaneous reactive power $\boldsymbol{q}$. A dc capacitor for energy storage during transient is sufficient.

2.6.2 Scalar Instantaneous Reactive Power

Equation (2.41) defines a three-dimensional vector $\boldsymbol{q}$ representing instantaneous reactive power. However it is also useful to have a scalar quantity q representing instantaneous reactive power of the overall three-phase system. A definition of this scalar may be chosen from the following alternatives.

(*i*) Norm of $\boldsymbol{q}$ i.e. $q = \|q\| = \sqrt{q_a^2 + q_b^2 + q_c^2}$

(*ii*) Algebraic sum of components of $\boldsymbol{q}$ i.e.

$$q = q_{sum} = q_a + q_b + q_c \tag{2.48}$$

In Section 2.7 of this chapter the alternative (*ii*) i.e. (2.48) is chosen. An advantage of this representation is that it can indicate the polarity of the instantaneous reactive power unlike $\|\boldsymbol{q}\|$ which is always positive. Further the algebraic sum preserves the division into an average and an alternative component. From (2.48) and since reactive power has two parts (average and alternating), we get

$q_j = \bar{q}_j + \tilde{q}_j$ for $j = a,b,c$. Then

$$q = q_{sum} = \bar{q} + \tilde{q} \tag{2.49}$$

where $\bar{q} = \sum_{j=a,b,c} q_j$ and $\tilde{q} = \sum_{j=a,b,c} \tilde{q}_j$

2.6.3 Instantaneous Active and Reactive Powers under Orthogonal Transformation

The 3-phase voltages and current, v_a, v_b, v_c and i_a, i_b, i_c may be transformed into the $\alpha - \beta - 0$ by a transformation matrix $\boldsymbol{C}$

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_o \end{bmatrix} = \boldsymbol{C} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} v_\alpha \\ v_\beta \\ v_o \end{bmatrix} = \boldsymbol{C} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.50}$$

If C is orthogonal i.e. $C^{-1} = C^t$ then

$$p = v_{abc}^t \cdot i_{abc} = (C^{-1} v_{\alpha\beta 0})^t \cdot (C^{-1} i_{\alpha\beta 0}) = v_{\alpha\beta 0}\, i_{\alpha\beta 0} \tag{2.51}$$

The instantaneous real power remains unchanged if transformation matrix is orthogonal. The instantaneous reactive power vector in the two systems are defined by,

$$q_{abc} = v_{abc} \times i_{abc} \tag{2.52}$$

and

$$q_{\alpha\beta 0} = v_{\alpha\beta 0} \times i_{\alpha\beta 0} \tag{2.53}$$

where suffixes 'abc' and '$\alpha\beta 0$' denote the corresponding coordinates. For an orthogonal matrix C

$$q_{\alpha\beta 0} = C\, q_{abc} \tag{2.54}$$

A popular choice of the orthogonal transformation matrix C is

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & -\sqrt{3}/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}$$

The basic definitions on the $\alpha - \beta - 0$ domain can be written by analogy from a-b-c domain. Thus,

$$p = v_\alpha\, i_\alpha + v_\beta\, i_\beta + v_o\, i_o \tag{2.55}$$

2.6.4 Instantaneous Active and Reactive Powers Using Instantaneous Symmetrical Components

Using theory of instantaneous symmetrical components [67], we can express source voltage and currents in terms of sequence components by inverse of the transformation used in (2.24)-(2.25). We can therefore write

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} v_{a0} \\ v_{a1} \\ v_{a2} \end{bmatrix} \tag{2.60}$$

A similar transformation can be used for currents

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} i_{a0} \\ i_{a1} \\ i_{a2} \end{bmatrix} \tag{2.61}$$

Using (2.40)-(2.41), and (2.60)-(2.61), we can compute the active and reactive powers in terms of instantaneous symmetrical components. On simplifying, we get,

$$p = v_a i_a + v_b i_b + v_c i_c = v_{a0}\, i_{a0} + 2\,Re\left(v_{a1}\, i_{a1}^*\right) \tag{2.62}$$

$$\begin{aligned} q = \begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} &= \begin{bmatrix} \begin{vmatrix} v_b & v_c \\ i_b & i_c \end{vmatrix} & \begin{vmatrix} v_c & v_a \\ i_c & i_a \end{vmatrix} & \begin{vmatrix} v_a & v_b \\ i_a & i_b \end{vmatrix} \end{bmatrix}^t \\ &= -\frac{2}{\sqrt{3}}\, Im \begin{bmatrix} v_{a1}\, i_{a1}^* \\ v_{a1}\, i_{a1}^* \\ v_{a1}\, i_{a1}^* \end{bmatrix} - \frac{2}{\sqrt{3}}\, v_{a0}\, Im \begin{bmatrix} i_{a1} \\ i_{a1}\, e^{-j2\pi/3} \\ i_{a1}\, e^{+j2\pi/3} \end{bmatrix} + \frac{2}{\sqrt{3}}\, i_{a0}\, Im \begin{bmatrix} v_{a1} \\ v_{a1}\, e^{-j2\pi/3} \\ v_{a1}\, e^{+j2\pi/3} \end{bmatrix} \end{aligned} \tag{2.63}$$

where, Re denotes the real components and Im the imaginary components and '*' the conjugate of a complex quantity. The Equations (2.62)-(2.63) are very useful in explaining the compensator performance when the system voltages are unbalanced.

Similarly, the instantaneous scalar reactive power is given by

$$\begin{aligned} q_{sum} &= q_a + q_b + q_c \\ &= -2\sqrt{3}\, Im\left(v_{a1}\, i_{a1}^{*}\right) \end{aligned} \tag{2.64}$$

It is seen from (2.63) that the terms containing v_{a0} and i_{a0} do not contribute to the q_{sum}. In general, q_{sum} has a dc component, $\bar{q}_{sum}$, and a double fundamental frequency component, $\tilde{q}_{sum}$. Thus first term of (2.63) only contributes to the average reactive power, $\bar{q}_{sum}$.

2.7 PROPOSED GENERAL ALGORITHM BASED ON GENERALIZED PQ THEORY

In general, the active and reactive powers have two components i.e. average and oscillating as given by (2.15)-(2.16). In the following discussion, the subscripts *'s', 'l' and 'f'* will denote the source, load and compensator (filter) respectively. For example $\bar{p}_l$ denotes the average load power, $\tilde{q}_s$ denotes the zero mean oscillating instantaneous reactive source power vector and i_l denotes the instantaneous load current vector. The averaging of powers is usually carried out over one half cycle of system voltage (10 ms for a 50 Hz system).

Using the definitions given in Section 2.6, it is possible to write the instantaneous vector of filter reference currents in terms of filter reactive power (q_f) and active power (p_f) as

$$i_f^{*} = i_{fq}^{*} + i_{fp}^{*} = \frac{q_f \times v_s}{v_s^t \cdot v_s} + \frac{p_f v_s}{v_s^t \cdot v_s} \tag{2.65}$$

Similarly, the instantaneous source current vector is written in terms of the source reactive power (q_s) and active power (p_s) as

$$i_s = i_{sq} + i_{sp} = \frac{q_s \times v_s}{v_s^t \cdot v_s} + \frac{p_s v_s}{v_s^t \cdot v_s} \tag{2.66}$$

We consider the general schematic diagram of the compensated system shown in Fig. 2.1 in which, the compensator is realized with three ideal current sources i^*_{fa}, i^*_{fb} and i^*_{fc}. Applying KCL at three nodes of the PCC and expressing currents in vector form, we get

$$\boldsymbol{i}^*_f = \boldsymbol{i}_l - \boldsymbol{i}_s \tag{2.67}$$

We expand vector $\boldsymbol{i}_s$ in (2.67) by applying (2.66) and definition of cross product similar to (2.41). This gives the following time domain expressions for filter reference currents.

$$\left.\begin{aligned} i^*_{fa} &= i_{la} - i_{sa} = i_{la} - \frac{1}{\sum_{j=a,b,c} v^2_{sj}}\left(p_s v_{sa} + q_{sb} v_{sc} - q_{sc} v_{sb}\right) \\ i^*_{fb} &= i_{lb} - i_{sb} = i_{lb} - \frac{1}{\sum_{j=a,b,c} v^2_{sj}}\left(p_s v_{sb} + q_{sc} v_{sa} - q_{sa} v_{sc}\right) \\ i^*_{fc} &= i_{lc} - i_{sc} = i_{lc} - \frac{1}{\sum_{j=a,b,c} v^2_{sj}}\left(p_s v_{sc} + q_{sa} v_{sb} - q_{sb} v_{sa}\right) \end{aligned}\right\} \tag{2.68}$$

Equations (2.68) for reference filter currents are equivalent to (2.65), but they use the desired source powers instead of filter powers. Considering filter current sources (Fig. 2.1) to be ideal, the appropriate selection of source power terms, p_s and q_{sa}, q_{sb}, q_{sc} based on load powers gives different kinds of compensation schemes. The implementation of these schemes involves continuous measurement of system voltages and load currents and real time calculation of various active and reactive load powers.

2.7.1 Various Compensation Schemes and Their Characteristics Based on General Algorithm

The various compensating schemes are tabulated in Table. 2.1 for different choices of instantaneous active and reactive powers of the source.

Table 2.1 Instantaneous active and reactive powers for compensator and source

Power details / Case	Active and reactive powers drawn from source				Active and reactive powers supplied by compensator	
	p_s	q_{sa}	q_{sb}	q_{sc}	p_f	q_f
1.	$\bar{p}_l$	0	0	0	$\tilde{p}_l$	q_l
2.	$\bar{p}_l$	$\beta\bar{q}_l/3$	$\beta\bar{q}_l/3$	$\beta\bar{q}_l/3$	$\tilde{p}_l$	$q_l-\beta\bar{q}_{lavg}$
3.	p_l	0	0	0	0	q_l
4.	p_l	$\bar{q}_l/3$	$\bar{q}_l/3$	$\bar{q}_l/3$	0	$q_l-\bar{q}_{lavg}$
5.	$\bar{p}_l$	$\tilde{q}_l/3$	$\tilde{q}_l/3$	$\tilde{q}_l/3$	$\tilde{p}_l$	$q_l-\tilde{q}_{lavg}$
6.	$\bar{p}_l$	$q_l/3$	$q_l/3$	$q_l/3$	$\tilde{p}_l$	q_l-q_{lavg}
7.	p_l	$\tilde{q}_l/3$	$\tilde{q}_l/3$	$\tilde{q}_l/3$	0	$q_l-\tilde{q}_{lavg}$

The various powers shown in table are defined as follows. As per (2.41) and (2.16)

$$\boldsymbol{q}_l=\bar{\boldsymbol{q}}_l+\tilde{\boldsymbol{q}}_l=\begin{bmatrix}q_{la}\\q_{lb}\\q_{lc}\end{bmatrix}=\begin{bmatrix}\bar{q}_{la}\\\bar{q}_{lb}\\\bar{q}_{lc}\end{bmatrix}+\begin{bmatrix}\tilde{q}_{la}\\\tilde{q}_{lb}\\\tilde{q}_{lc}\end{bmatrix} \tag{2.69}$$

Similarly as per (2.40) and (2.15)

$$p_l=\bar{p}_l+\tilde{p}_l \tag{2.70}$$

As defined in Sub-section 2.6.2, the algebraic sum $q_l=q_{l\,sum}=q_{la}+q_{lb}+q_{lc}$ has been used as the scalar instantaneous reactive power in the Table 2.1. Therefore the scalar instantaneous reactive powers $\bar{q}_l$ and $\tilde{q}_l$ are average and zero mean oscillating values over three phases are,

$$\left.\begin{aligned}\bar{q}_l&=\bar{q}_{l\,sum}=(\bar{q}_{la}+\bar{q}_{lb}+\bar{q}_{lc})\\\tilde{q}_l&=\tilde{q}_{l\,sum}=(\tilde{q}_{la}+\tilde{q}_{lb}+\tilde{q}_{lc})\end{aligned}\right\} \tag{2.71}$$

In Table 2.1, the average reactive power vector is

$$q_{lavg} = \begin{bmatrix} q_l/3 \\ q_l/3 \\ q_l/3 \end{bmatrix} = \begin{bmatrix} \bar{q}_l/3 \\ \bar{q}_l/3 \\ \bar{q}_l/3 \end{bmatrix} + \begin{bmatrix} \tilde{q}_l/3 \\ \tilde{q}_l/3 \\ \tilde{q}_l/3 \end{bmatrix} = \bar{q}_{lavg} + \tilde{q}_{lavg} \tag{2.72}$$

In Table 2.1 (Case 2), β is a factor (usually between 0 and 1) which decides the desired power factor of the source. The relation between β and the desired phase shift ϕ between source current and source voltage is given by

$$\beta = \frac{\bar{p}_l}{\bar{q}_l/\sqrt{3}} \tan\phi \tag{2.73}$$

In (2.73), the factor of $\sqrt{3}$ results due to particular definition of scalar load average reactive power, $\bar{q}_l$, in (2.71).

It is to be noted that the expressions (2.68) for compensator reference currents are very general in nature. Several algorithms for reference current generation can be obtained by choosing the source powers in these expressions. For example, if it is desired that the compensated source currents are balanced and have a certain phase angle with the supply voltages, the choice for the source active and reactive powers are as follows.

$$p_s = \bar{p}_l \text{ and } q_{sa} = q_{sb} = q_{sc} = \beta\,\bar{q}_l/3 \tag{2.74}$$

Substituting these values of source powers in (2.68), we get

$$\left.\begin{aligned} i^*_{fa} &= i_{la} - i_{sa} = i_{la} - \frac{\bar{p}_l v_{sa} + \beta\,\bar{q}_l (v_{sc} - v_{sb})/3}{\sum_{j=a,b,c} v_{sj}^2} \\ i^*_{fb} &= i_{lb} - i_{sb} = i_{lb} - \frac{\bar{p}_l v_{sb} + \beta\,\bar{q}_l (v_{sa} - v_{sc})/3}{\sum_{j=a,b,c} v_{sj}^2} \\ i^*_{fc} &= i_{lc} - i_{sc} = i_{lc} - \frac{\bar{p}_l v_{sb} + \beta\,\bar{q}_l (v_{sb} - v_{sa})/3}{\sum_{j=a,b,c} v_{sj}^2} \end{aligned}\right\} \tag{2.75}$$

The expressions for compensator currents (2.75) are similar to expressions (2.32) given in compensation based on the theory of instantaneous symmetrical components in Section 2.5. For unity power factor operation β is set to zero in (2.75). For non-unity, the relation between β in (2.75) and γ in (2.32) is given as,

$$\gamma = -\frac{\bar{q}_l}{3\bar{p}_l}\beta \tag{2.76}$$

Several other compensating schemes obtained by choosing appropriate values of source powers in (2.68) are shown in Table 2.1. Equations similar to (2.75) can be obtained for each of these cases.

2.7.2 Operation of Ideal Compensator for Balanced Supply Voltages: Simulation and Experimental Verification

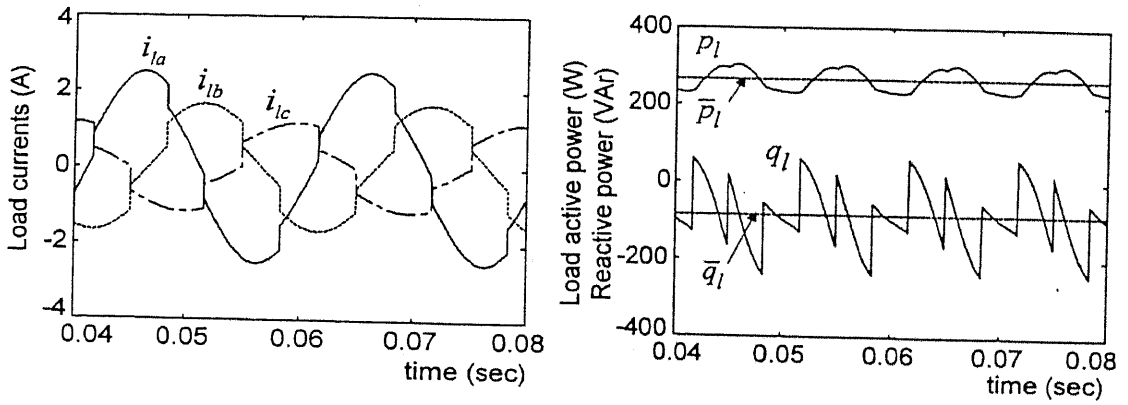
The various compensation schemes given in Table 2.1 have been simulated using MATLAB. The system parameters chosen are given in Table 2.2. For these simulation studies and experimental results we assume an ideal inverter. This implies that we have a current source that can accurately follow the reference currents generated. Studies with non-ideal inverter and DSTATCOM topologies will be discussed in subsequent chapters.

Table 2.2 System parameters

System Parameters	Values
System frequency	50 Hz
Source voltages	100 V (peak)
Load	◆ $Z_a = 53\angle 22^o\,\Omega$, $Z_b = 96\angle 0^o\,\Omega$, $Z_c = 182\angle 28^o\,\Omega$ ◆ Three-phase full bridge diode rectifier drawing dc load current of 0.625 A

For given system voltages and load configuration, the steady state load currents are computed. The load currents i_{la}, i_{lb}, i_{lc} have been plotted in Fig. 2.9 (a). Then, the power terms p_l, and $\boldsymbol{q}_l$ (whose components are q_{la}, q_{lb} and q_{lc}) are computed using (2.40) and (2.41) respectively and plotted in Fig. 2.9 (b). Using the samples of p_l, and $\boldsymbol{q}_l$, we

compute $\bar{p}_l$ and $\bar{q}_l$ using moving average filter over half cycle [46]. This choice is due to the fact that the load real and reactive powers have a fundamental frequency of 100 Hz. This also has the effect that low frequency sub-harmonics in load currents will result in low frequency modulation of source current. However any attempt to eliminate this low frequency modulation will adversely affect the dynamic performance of the compensator, since the averaging time will have to be increased. Scalar average reactive power of the load, $\bar{q}_l$, is computed using (2.71) and is –ve for lagging loads. Vector $\tilde{q}_l$ is computed by subtracting $\bar{q}_l$ from q_l using (2.69). Thus, the power terms p_l, $\bar{p}_l$, q_l, $\bar{q}_l$ and $\tilde{q}_l$ are known and are substituted appropriately for p_s, q_{sa}, q_{sb} and q_{sc} in (2.68) to generate filter reference currents according to Table 2.1 so as to achieve different compensation schemes.



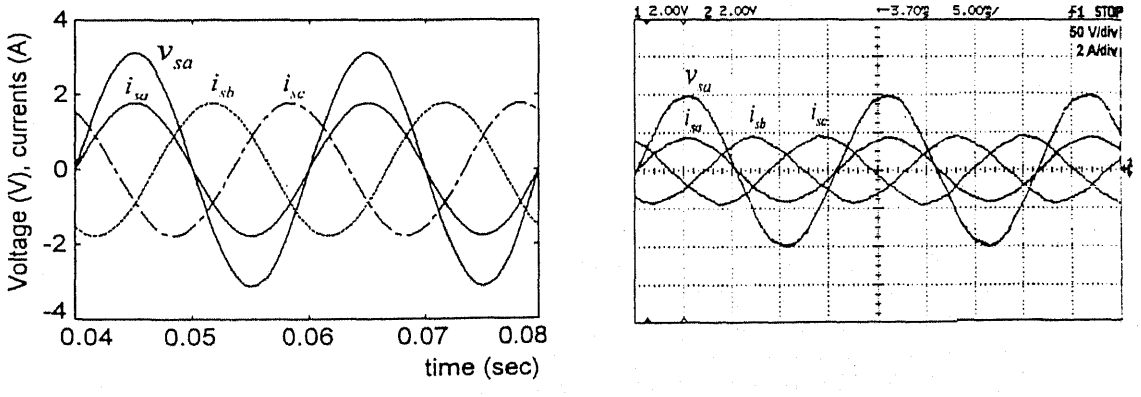
(a) (b)

Fig. 2.9 (a) Load currents and (b) Load active and reactive powers

The simulation results have been verified on an experimental set-up, given in Appendix-A, with parameters same as those given for simulation. The diode bridge converter has been loaded with a large inductance (270 mH) to obtain nearly constant load current. Experimental generation of ideal source currents is achieved by implementing the compensation algorithm (2.68) on an IBM compatible PC. Hall effect voltage and current transducers (Appendix C) are used to obtain samples of voltages and load currents in the range of ± 2.5 V. The PC acquires these quantities through the data acquisition card, NuDAQ 9118 DG (Appendix B) [87]. From these values the desired source active and reactive powers as per Table 2.1 are computed and substituted in (2.68). The real time

computation of (2.68) is performed through a program written in C language. This gives the instantaneous values of compensator reference currents. If the compensator is assumed to be ideal, these reference currents (i^*_{fa}, i^*_{fb}, i^*_{fc}) are identical to the actual compensator current (i_{fa}, i_{fb}, i_{fc}) respectively (Fig. 2.1). Therefore, the ideal source currents can be computed as the difference ($i_l - i^*_f$) as per (2.67). Accordingly, computed compensator current values are subtracted from the corresponding load current values to generate the ideal source currents. The simulation and experimental source currents are shown in Figs. 2.10-2.16. In these figures a scaled version (1/32) of the source voltage in phase-*a* is also plotted such that source current behavior vis-a-vis the source voltage can be seen. The seven cases of compensation (Table 2.1) have been considered here.

Case 1: The compensator supplies the total reactive power (q_l) and also the zero mean oscillating active power ($\tilde{p}_l$) of the load. The source supplies only the average load power ($\bar{p}_l$) The simulated and experimental results are shown in Fig. 2.10 (a) and (b) respectively. It is seen from these figures that compensated source currents are in phase with their respective source voltages, and they are balanced sinusoids.

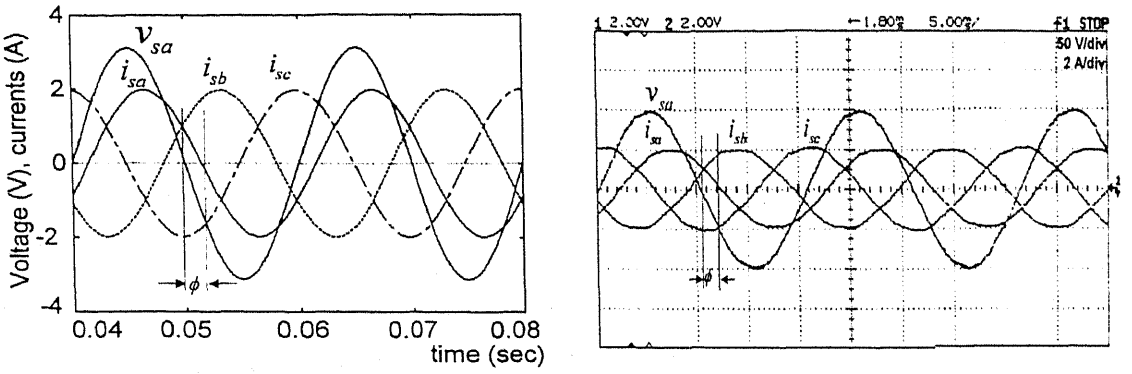


(a) (b)

Fig. 2.10 Source currents with $p_s = \bar{p}_l$, $q_s = 0$ (Case 1): (a) Simulated (b) Experimental

Case 2: Case 1 is repeated except the source supplies a part of or more than total average reactive power ($\bar{q}_l$) of the load. This gives a desired power factor of the source. For instance, if desired power factor is 0.95 lag ($\phi = 26^\circ$), β calculated from (2.73) is 2.72.

This phase lag is also seen from Fig. 2.11 (a) and (b). In order to supply a part of total average reactive power β can be varied from 0 to 1. The source power factor can even be made leading by choosing negative values of β.

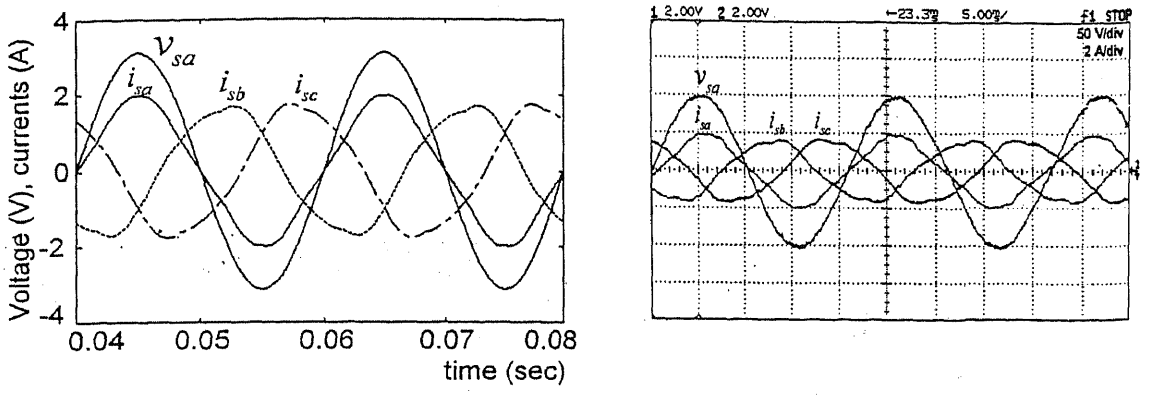


(a) (b)

Fig. 2.11 Source currents with $p_s = \bar{p}_l$, $q_s = \beta\, \bar{q}_{lavg}$ (Case 2): (a) Simulated (b) Experimental

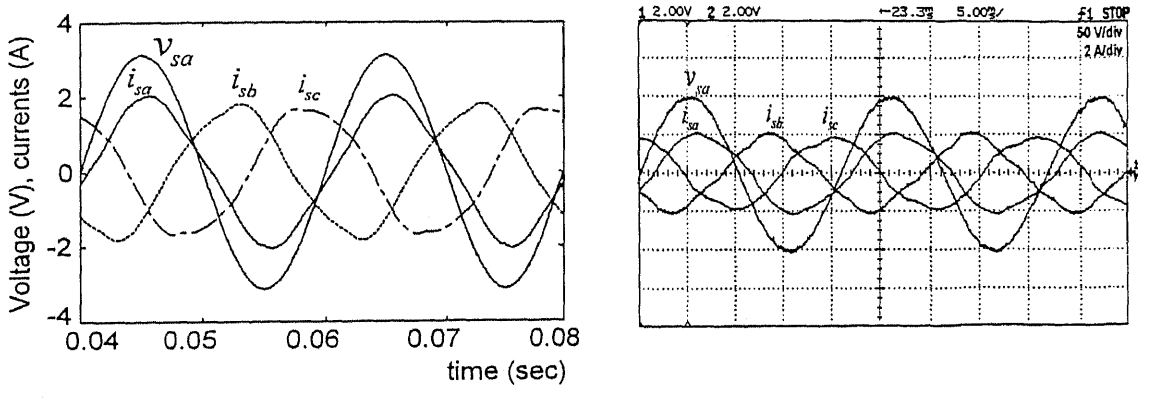
Case 3: The compensator supplies the total reactive power (q_l) while the source supplies the total active power (p_l) of the load. The simulated and experimental results are shown in Fig. 2.12 (a) and (b) respectively. It is observed that though the fundamentals of source currents are in phase with the respective supply voltages, they are not sinusoidal. The reason for this is that unlike cases 1 and 2, the zero mean oscillating active load power is also derived from the source.

Case 4: The source supplies the average reactive power ($\bar{q}_l$) and total active power (p_l) of the load, while the compensator supplies the zero mean oscillating reactive power of the load. In Fig. 2.13 (a) and (b), the source current waveforms are similar in shape to those of case 3. However, the fundamental components of phase currents are lagging with respect to their source voltages. The waveforms can also be compared with case 2, where the waveforms are smoother because $\tilde{p}_l$ has been compensated.



(a) (b)

Fig. 2.12 Source currents with $p_s = p_l$, $q_s = 0$ (Case 3): (a) Simulated (b) Experimental



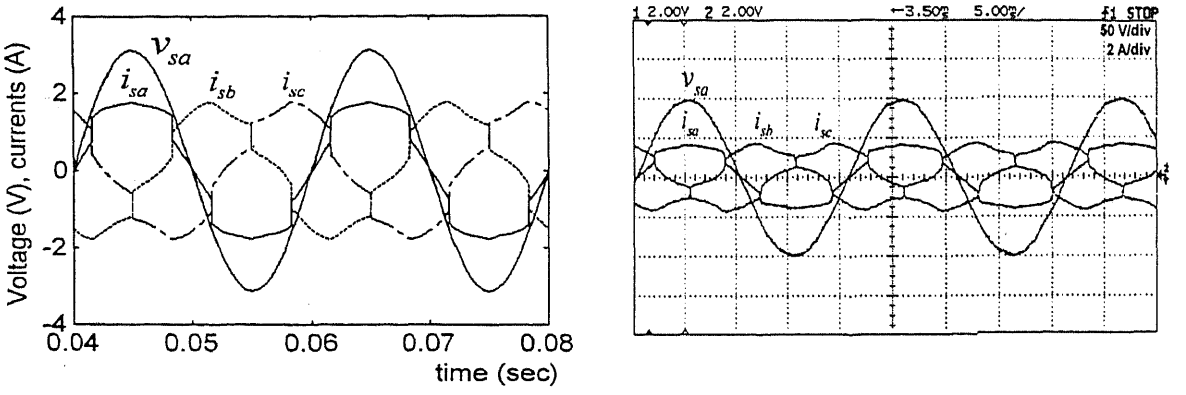
(a) (b)

Fig. 2.13 Source currents with $p_s = p_l$, $q_s = \bar{q}_{lavg}$ (Case 4): (a) Simulated (b) Experimental

Case 5: The source supplies powers $\tilde{q}_l$ and $\bar{p}_l$. The compensator supplies the remaining powers. The results are shown in Fig. 2.14 (a) and (b), where the fundamentals of source currents are seen to be in phase with voltages. The source currents are unbalanced and non-sinusoidal due to supply of $\tilde{q}_l$ from the source.

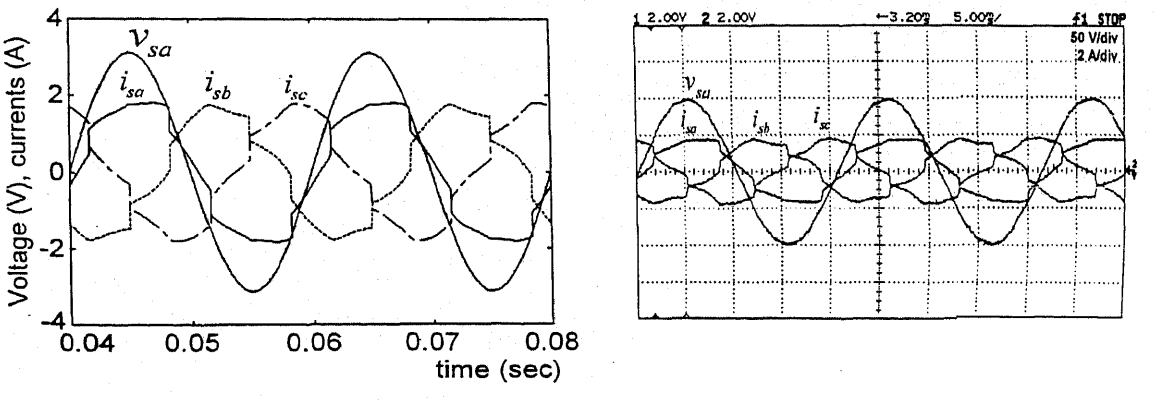
Case 6: The compensator supplies only the zero mean oscillating active power ($\tilde{p}_l$) of the load and the remaining load power is supplied by the source. This case arises if we want to suppress the mechanical vibrations in the prime movers arising due to supply of $\tilde{p}_l$ [71].

The source currents, shown in Fig. 2.15 (a) and (b), are unbalanced and non-sinusoidal. The fundamental components of currents also show a phase shift with respect to the source voltages.



(a) (b)

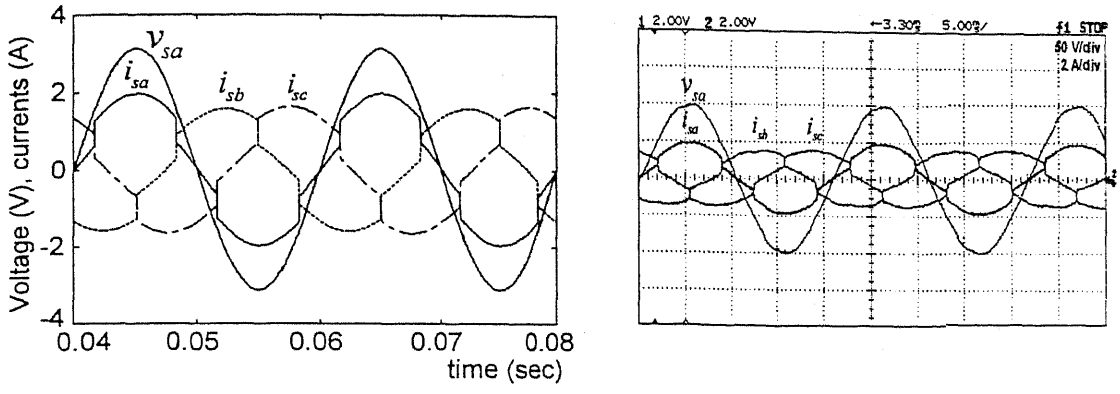
Fig. 2.14 Source currents with $p_s = \bar{p}_l$, $q_s = \tilde{q}_{lavg}$ (Case 5): (a) Simulated (b) Experimental



(a) (b)

Fig. 2.15 Source currents with $p_s = \bar{p}_l$, $q_s = q_{lavg}$ (Case 6): (a) Simulated (b) Experimental

Case 7: In this case, the source supplies the total active power (p_l) and reactive power ($\tilde{q}_l$), while rest of the power of load comes from the compensator. The simulated and experimental results are shown in Fig. 2.16 (a) and (b) respectively.



(a) (b)

Fig. 2.16 Source currents with $p_s = p_l$, $q_s = \tilde{q}_{lavg}$ (Case 7): (a) Simulated (b) Experimental

Thus we can make the compensator to take action on any of the power terms $\bar{q}_l$, $\tilde{q}_l$ and $\tilde{p}_l$, or their various combinations. However the average load power $\bar{p}_l$ and losses in a real compensator always come from the source. While we can make several other combinations, the most commonly used combinations (Cases 1, 2, 3) have been included above. The simulation for the Cases 2, 3, 4 and 6 in Table 2.1, using the *pq* theory, has been reported in [71]. For these cases, the simulated results given above using generalized instantaneous reactive power theory are found to be similar.

The different compensation schemes given in Table 2.1 give rise to different characteristics. Based on above simulation results, the effects of compensation for each case are summarized in Table 2.3. In Table 2.3, UPF and UDF stand for unity power factor and unity displacement factor respectively. Displacement factor is related to the power factor angle between the fundamental waveforms of the distorted voltage and current signals. It is observed from simulation results that in several cases the source currents are unbalanced and have notches. The unbalance results when the source supplies zero mean oscillating powers $\tilde{p}_l$, $\tilde{q}_{lavg}$. The notches result from discontinuities in $\tilde{p}_l$ and $\tilde{q}_l$ due to the ideal rectifier diode bridge. There is a possibility of using the source reactive power terms (q_{la},

q_{lb}, q_{lc}) and ($\tilde{q}_{la}$,$\tilde{q}_{lb}$, $\tilde{q}_{lc}$) instead of $q_l/3$ and ($\tilde{q}_l/3$) respectively in Table 2.1, cases 5-7 [48]. However, this choice is not considered as it results in more unbalance and distortion in waveforms of compensated sources currents than those shown in Figs. 2.14–2.16.

Table 2.2 Various compensation strategies and their characteristics

Case	Remarks on effects of compensation on source currents	Fig. No.
1.	UPF, smooth, sinusoidal balanced	2.10 (a)-(b)
2.	Non-UPF, balanced sinusoidal	2.11 (a)-(b)
3.	UDF, notches, unbalanced	2.12 (a)-(b)
4.	Non-UDF, notches, unbalanced	2.13 (a)-(b)
5.	UDF, notches, unbalance	2.14 (a)-(b)
6.	Non-UDF, notches, unbalanced	2.15 (a)-(b)
7.	UDF, notches, unbalanced	2.16 (a)-(b)

2.8 SHUNT COMPENSATION UNDER UNBALANCED SOURCE VOLTAGES

The *pq* theory (Section 2.4) gives effective operation and good performance under balanced system voltages. However, when the voltages are significantly unbalanced the direct application of this theory will result in large error [61]. Similarly, the compensation algorithm (2.32) based on the theory of instantaneous symmetrical components assumes balanced sinusoidal system voltages. Taking voltage unbalance into account, for three-phase star connected load the algorithm given in (2.31) can be directly used (for unity power factor γ is zero).

Using this algorithm, it can be easily shown that compensated currents are in phase with source voltages but are distorted and their magnitudes are not equal. The algorithm produces reference compensator currents which satisfy conditions, $\sum_{j=a,b,c} i_{sj} = 0$, $p_s = \bar{p}_l$ and $q_s = 0$.

The distortion in the compensated source currents arises due to the fact that the unbalanced voltages can not supply constant average load power with balanced sinusoidal currents. Therefore the computed source currents are suitably distorted to obtain constant power from unbalanced source voltages.

We start our discussion with simulated results that are presented for unbalanced source voltages. The distortion in source currents is explained using powers expressed in instantaneous symmetrical components of voltage and current. Then a modified algorithm based on (2.68) is proposed. An alternate algorithm is also proposed for unity power factor operation with unbalanced source voltages. The simulation and experimental results are presented with ideal inverter.

2.8.1 Operation of Ideal Compensator for Unbalanced Supply Voltages

The following magnitude and phase unbalance in supply voltages has been considered.

$$v_{sa} = 80\sin 100\pi t \text{ V},$$
$$v_{sb} = 100\sin(100\pi t - 2\pi/3 - \pi/6) \text{ V}$$
$$v_{sc} = 65\sin(100\pi t + 2\pi/3) \text{ V}$$

The load configuration and other system parameters are same as those given in Table 2.2. The unbalanced source voltages are plotted in Fig. 2.17. The load currents of Fig. 2.9 will change accordingly. Considering unity power factor operation, (Case 1 with $\beta = 0$ in Table 2.1). The load active power p_l is shown in Fig. 2.18. The average load power ($\bar{p}_l$) is 198 W.

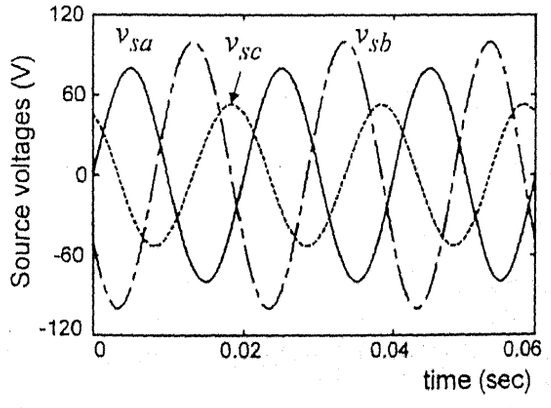


Fig. 2.17 Unbalance source voltages

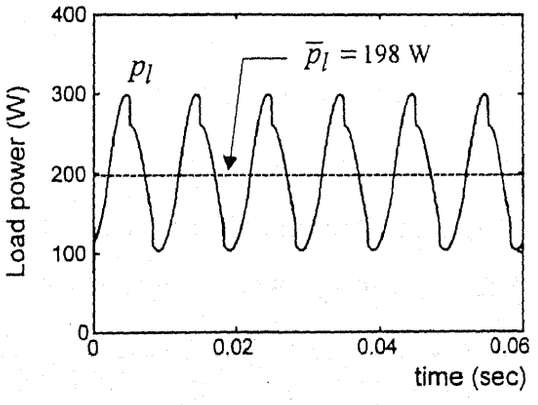


Fig. 2.18 Load power

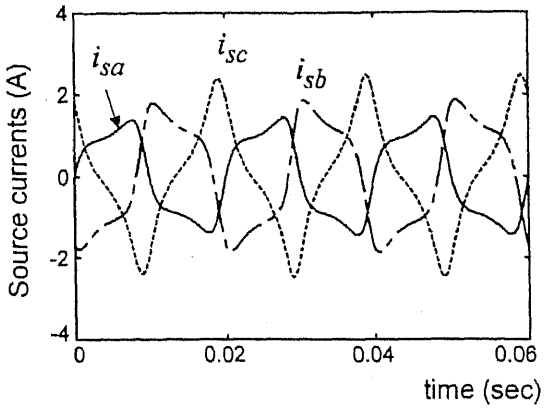


Fig. 2.19 Distorted compensated source currents

For a balanced three-phase system, with three phase balanced sinusoidal voltages and balanced sinusoidal currents, the three phase instantaneous active power is always a constant. Similarly, the three instantaneous reactive powers, q_{sa}, q_{sb}, q_{sc} are also constant.

In a compensated system, when source voltages are balanced, $v_{a0} = 0$. However, the load currents may be balanced or unbalanced. But due to compensator action, the source currents become balanced, and therefore $i_{a0} = 0$. Consequently, the first term of (2.62) and second and third terms of (2.63) are zero and p_s and $\boldsymbol{q}_s$ become constant. Thus, the compensated system becomes a three phase balanced system.

Now when voltages are unbalanced, the unbalance is passed on to the compensator control algorithm (2.68) and results in a particular kind of compensation. The compensator does satisfy the overall conditions imposed on it by the algorithm (2.68), i.e. $p_s = \bar{p}_l$ and each component of $\boldsymbol{q}_s$ is zero. Since the voltages are unbalanced, and we constrain the source to supply a constant power, p_s, equal to the average load power, $\bar{p}_l$, the currents distort from the sinusoidal as shown in Fig. 2.19. As a consequence of voltage unbalance, both v_{a0} and i_{a0} are non-zero, time varying and i_{a0} is also non-sinusoidal. Thus in (2.62), the first term, i.e. $v_{a0}\, i_{a0}$ becomes non-sinusoidal whose ac part is equal and opposite to ac part of the second term. Similarly, the second and third terms in (2.63) in each phase yield

non-sinusoidal variation. These non-sinusoidal variations are measure of the distortion in source currents seen in Fig. 2.19. To overcome this problem the algorithm (2.68) is modified as described in the following sub-section.

2.8.2 Modified Algorithm for Unbalanced Voltages

Let there be unbalance in magnitudes and in phase angles of the supply voltages, i.e.

$$\left.\begin{aligned} v_{sa} &= V_{sma}\sin\omega t \\ v_{sb} &= V_{smb}\sin(\omega t - 2\pi/3 + \theta_b) \\ v_{sc} &= V_{smc}\sin(\omega t + 2\pi/3 + \theta_c) \end{aligned}\right\} \tag{2.77}$$

In (2.77), the magnitudes V_{sma}, V_{smb}, V_{smc} are unequal. The phase angles θ_b and θ_c contribute to the phase unbalance. The algorithm given in (2.68) is modified by using a fictitious set of voltages v'_{sa}, v'_{sb}, v'_{sc} in place of the real voltages v_{sa}, v_{sb}, v_{sc}, given by

$$\left.\begin{aligned} v'_{sa} &= V'_{sm}\sin\omega t \\ v'_{sb} &= V'_{sm}\sin(\omega t - 2\pi/3) \\ v'_{sc} &= V'_{sm}\sin(\omega t + 2\pi/3) \end{aligned}\right\} \tag{2.78}$$

The use of balanced voltages in the algorithm produces balanced compensated source currents as discussed in Section 2.6. For balanced compensated source currents, both sets of voltages given by (2.77) and (2.78) above, should yield equal average real power, $\bar{p}_s$. From this requirement, we obtain the magnitude V'_{sm} as,

$$V'_{sm} = \frac{1}{3}\left(v_{sa} + v_{sb}\alpha_b + v_{sc}\alpha_c\right) \tag{2.79}$$

where

$$\alpha_b = \frac{\cos(\phi + \theta_b)}{\cos\phi} \text{ and } \alpha_c = \frac{\cos(\phi + \theta_c)}{\cos\phi} \tag{2.80}$$

where, ϕ being the desired phase angle between the source voltage v_{sa} and the desired compensated source current i_{sa}. In the case of unbalance in magnitudes only i.e. $\theta_b = \theta_c =$

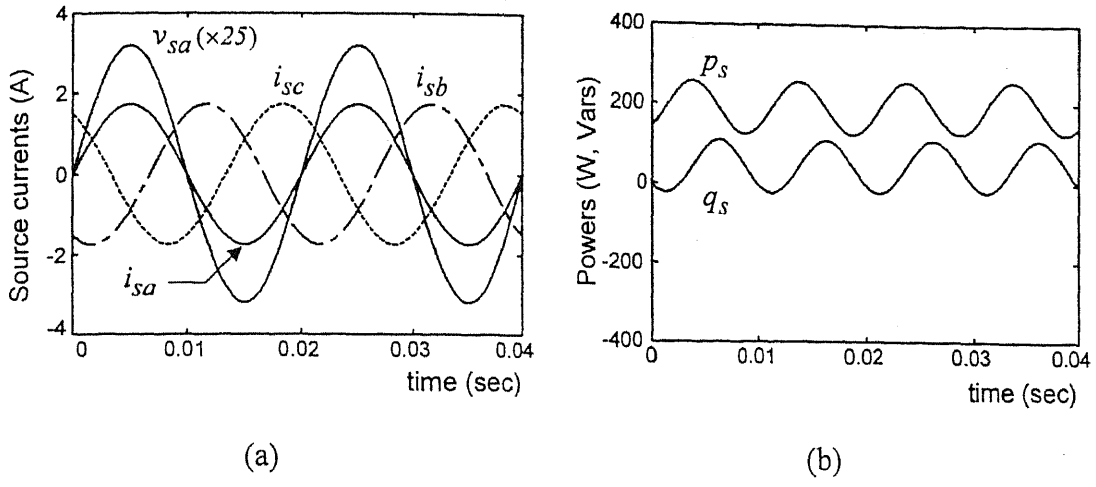
0, the factors α_b and α_c in (2.80) reduce to unity and consequently V'_{sm} is the average of the unequal magnitudes v_{sa}, v_{sb}, v_{sc}.

Based on above considerations, The modified algorithm for filter reference currents is as follows

$$\left.\begin{aligned} i^*_{fa} &= i_{la} - \frac{1}{\sum_{j=a,b,c} v'^2_{sj}}\left(p_s v'_{sa} + q_{sb} v'_{sc} - q_{sc} v'_{sb}\right) \\ i^*_{fb} &= i_{lb} - \frac{1}{\sum_{j=a,b,c} v'^2_{sj}}\left(p_s v'_{sb} + q_{sc} v'_{sa} - q_{sa} v'_{sc}\right) \\ i^*_{fc} &= i_{lc} - \frac{1}{\sum_{j=a,b,c} v'^2_{sj}}\left(p_s v'_{sc} + q_{sa} v'_{sb} - q_{sb} v'_{sa}\right) \end{aligned}\right\} \qquad (2.81)$$

The power terms in (2.81) are obtained from Case 1 in Table 2.1 and measured load powers by the same procedure as in the case of the balanced voltages as discussed in Sub-section 2.7.2. With this algorithm, considering the same parameters as in Table 2.2 and the same unbalance in source voltage as considered in Sub-section 2.8.1, the simulated results for unity power factor operation i.e. $\beta = 0$ are shown in the Fig. 2.20 (a) and (b). It is seen from Fig. 2.20 (a) that the compensated source currents obtained from the modified algorithm are balanced sinusoids, unlike the distorted waveforms of Fig. 2.19.

The above algorithm may be referred to as Equal Current Strategy. Similar strategies have been reported as Sinusoidal Current Source Strategy in [55] and Equal Current Criteria in [61]. However in [55], to find the fictitious balanced set of voltages for control algorithm, the complex $\alpha - \beta - 0$ transformations and elaborate computations are used. In [61] the synchronous detection method is used but it is limited to the case of unity power factor and magnitude unbalance only. The modified algorithm given above, using generalized theory is simple and considers unbalances in magnitudes and/or phase angles. The algorithm also provides the facility of setting the desired power factor angle, ϕ.



(a) (b)

Fig. 2.20 (a) Compensated source currents (b) Instantaneous active and reactive powers

It is to be noted that if we consider v'_{sa}, v'_{sb}, v'_{sc}, fictitious balanced supply voltages then the fictitious source would supply only average load power and no zero mean oscillating active and reactive power. But since the actual supply has unbalance in magnitudes, so the source supplies some constant mean oscillating active and reactive powers as shown in Fig. 2.20 (b).

2.8.3. An Alternate Algorithm for Unity Power Factor Operation

Equal Resistance Strategy has been reported in [61]. This strategy can also be realized using generalized algorithm (2.63) with appropriate choice of power terms p_s, q_{sa}, q_{sb} and q_{sc}. One way to remove the non-sinusoidal variations of the terms in (2.62) and (2.63) described above is to impose the following condition on the source currents

$$\frac{v_{sa}}{i_{sa}} = \frac{v_{sb}}{i_{sb}} = \frac{v_{sc}}{i_{sc}} = R_{eq} \tag{2.82}$$

Where R_{eq} is equivalent resistance of each phase as seen by the source. Using (2.24)-(2.25), and applying (2.82), it can be shown that $v_{a0} = i_{a0} R_{eq}$, $v_{a1} = i_{a1} R_{eq}$ and i_{a0} is sinusoidal. Therefore, the first term in (2.63) is zero by itself and second and third terms cancel in each phase. Hence the vector q_s and its components q_{sa}, q_{sb} and q_{sc} in (2.63) become zero. Further real power p_s (2.62) consists of a dc and a sinusoidal part in each

term. Because the compensated system is equivalent to a resistance in each phase, the power drawn from the source is given as,

$$p_s = \frac{\sum_{j=a,b,c} v_{sj}^2}{R_{eq}} \tag{2.83}$$

Using p_s from (2.83) and $q_{sa} = q_{sb} = q_{sc} = 0$, we get from (2.68)

$$\left.\begin{aligned} i_{fa}^* &= i_{la} - \frac{v_{sa}}{R_{eq}} \\ i_{fb}^* &= i_{lb} - \frac{v_{sb}}{R_{eq}} \\ i_{fc}^* &= i_{lc} - \frac{v_{sc}}{R_{eq}} \end{aligned}\right\} \tag{2.84}$$

To determine R_{eq}, the average value of p_s in (2.83) is equated to the average load power. This gives,

$$\bar{p}_s = \frac{\left\langle \sum_{j=a,b,c} v_{sj}^2 \right\rangle}{R_{eq}} = \bar{p}_l \tag{2.85}$$

where the symbol '< >' refers for the average value over half cycle. For sinusoidal voltages (with or without unbalance in magnitudes and phase angles), the following relation is true

$$\left\langle \sum_{j=a,b,c} v_{sj}^2 \right\rangle = \frac{\sum_{j=a,b,c} V_{smj}^2}{2} \tag{2.86}$$

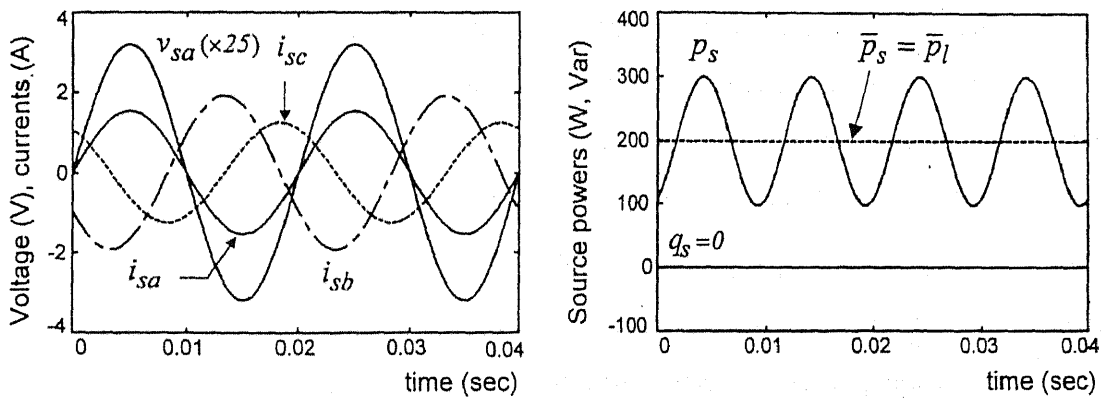
Using (2.86), the value of R_{eq} is given as,

$$R_{eq} = \frac{\sum_{j=a,b,c} V_{smj}^2}{2\bar{p}_l} \tag{2.87}$$

Where $V_{smj}\,(j = a,b,c)$ is the peak value of voltage in phase j. Substituting R_{eq} from (2.87), into (2.84) the instantaneous reference filter current vector is given as,

$$i_f^* = i_l - \frac{2\bar{p}_L}{\sum_{j=a,b,c} V_{smj}^2} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{2.88}$$

The performance of the improved compensator with voltage unbalance has been simulated using same parameters as in Table 2.2. The equation. (2.88) is used to generate the reference filter currents. The compensated source currents are shown in Fig. 2.21 (a). The active and reactive source powers are plotted in Fig. 2.21 (b).



(a) (b)

Fig. 2.21 (a) Source currents (b) Source and load powers of the improved compensation

Comparing the source current waveforms of Fig. 2.19 and Fig. 2.21 (a), it is seen that the later have no distortion. The source currents are purely sinusoidal and in phase with the respective phase voltages. The peak values of source currents are in proportion to the peaks of source voltages. This is achieved at the cost of drawing a particular value of zero mean oscillating active power from the source. This is seen in waveform of p_s, that it contains 100 Hz ac component in addition to $\bar{p}_l$ as shown in Fig. 2.21 (b). Thus if we use the

condition (2.82), we get improvement over the distorted source currents of Fig. 2.19 by redistribution of the zero mean oscillating active power between the source and the compensator. The source reactive power is zero by virtue of Equal Resistance Condition (2.82).

2.8.4. Experimental Results with Ideal Compensator

In this Sub-section, simulated results given in Sub-sections 2.8.2 and 2.8.3 are verified. The experimental parameters remain the same as given in Table 2.2. The unbalance in system source voltage is maintained approximately the same as considered in Sub-section 2.8.1. The unbalance in system source voltages is shown in Fig. 2.22. It is seen from the figure that source voltages are not perfectly sinusoidal as in simulation (Fig. 2.17). For these unbalanced source voltages, the load currents and load powers are shown in Fig. 2.23 and Fig. 2.24 respectively. When Case 1 of Table 2.1 in algorithm (2.63) is used as such, compensated source currents are highly distorted as discussed in details in Sub-section 2.8.1. Since source voltages are unbalanced, therefore source currents are also distorted in order to satisfy the source power constraints. These are shown in Fig. 2.25. The source powers are shown in Fig. 2.26. It is seen from the figure that the source power is flat and is equal to the average load power and source reactive power is equal to zero. Thus the algorithm still satisfies the source power constraints imposed on it.

Now the modified algorithm (2.88) is applied for load compensation under unbalanced voltages. The compensated source currents are shown in Fig. 2.27. It is seen from this figure that the compensated source currents are sinusoidal and balanced. In Fig. 2.28, waveforms of system voltage in phase-*a* and source current in phase-*a* are shown to indicate the phase relationship. The source current in phase-*b* will not be in phase with voltage of phase *b*, because phase-*b* voltage has shifted from ideal value of $4\pi/3$. It is for this reason the source active power p_s will not be flat and source reactive power q_s will not be zero. They will be oscillating of 100 Hz frequency. The source active and reactive powers are shown in Fig. 2.29. It is noted here that the average value of q_s is positive. This is due to the fact that the source current in phase-*b* is leading the phase-*b* source voltage.

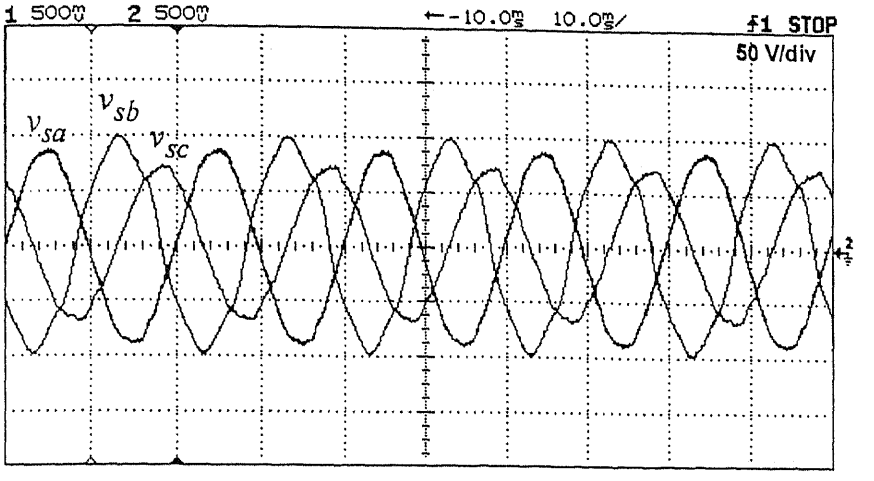


Fig. 2.22 Three-phase unbalanced system voltages

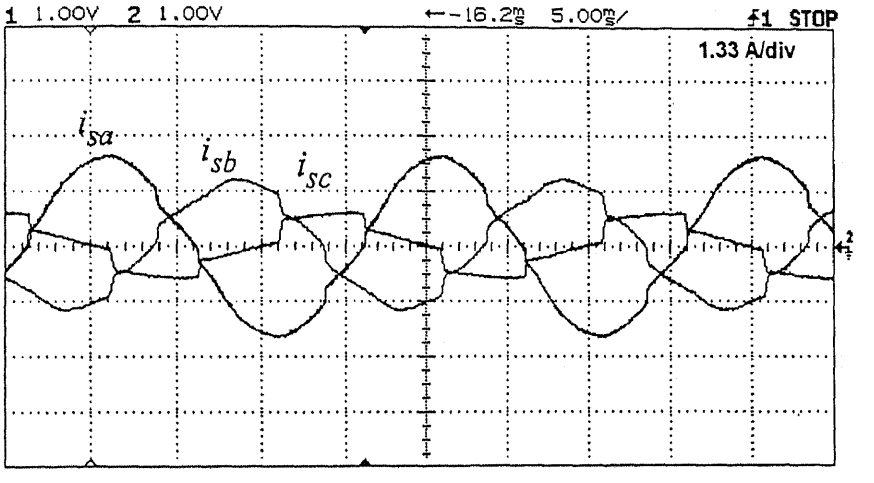


Fig. 2.23 Three-phase load currents

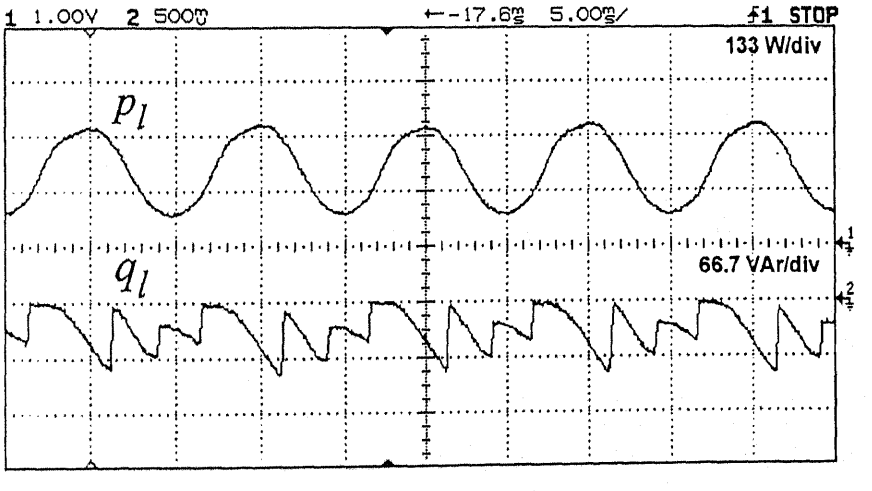


Fig. 2.24 Load active and reactive power

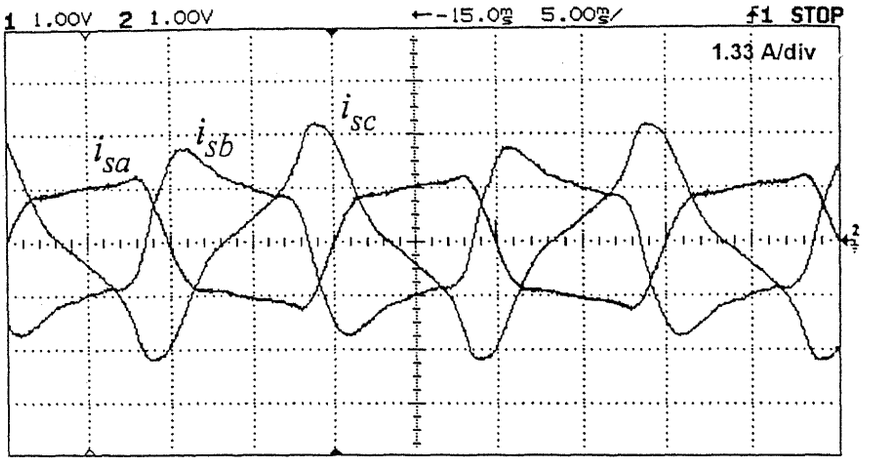


Fig. 2.25 Distorted source currents

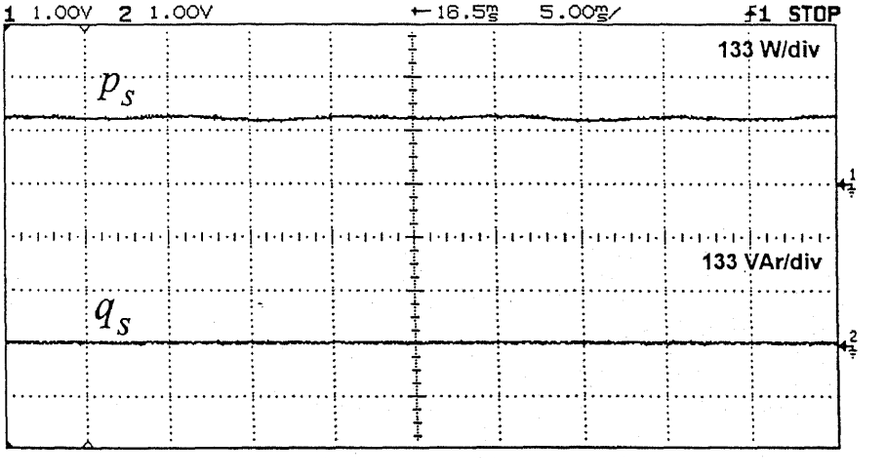


Fig. 2.26 Source active and reactive power

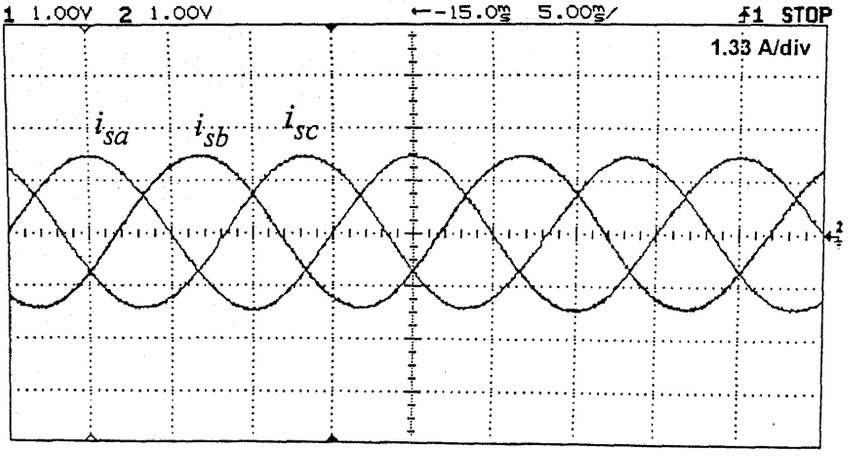


Fig. 2.27 Compensated source currents with modified algorithm

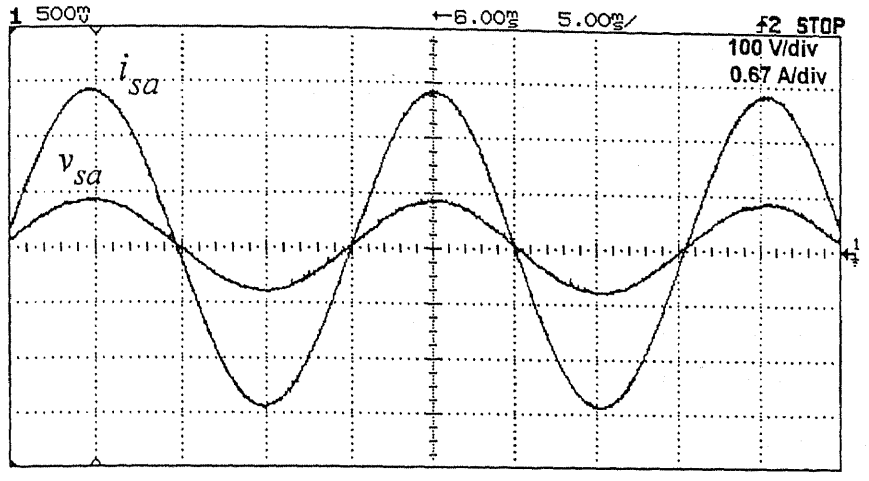


Fig. 2.28 Source current and voltage in phase-*a*

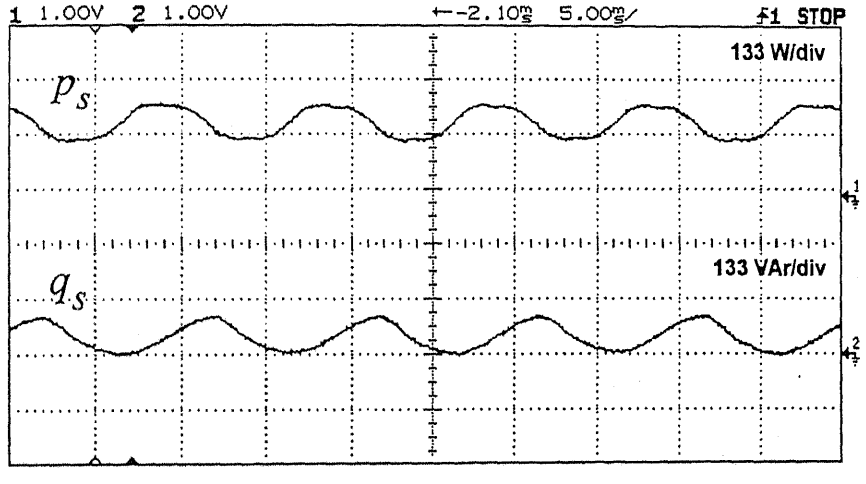


Fig. 2.29 Source active and reactive powers with modified algorithm

2.9 CONCLUSIONS

In this chapter, a general shunt algorithm has been proposed and applied to various kinds of compensation schemes. The real time expressions (2.68) for filter reference currents have been derived. These expressions are very general and true for balanced and unbalanced voltages and loads, with or without zero sequence components. Experimental results confirm that the algorithm (2.68) is computationally efficient. An implementation on a 350 MHz PC can easily compensate harmonics up to 3 kHz.

The proposed theory has been extended for unbalanced source voltage operation by introducing a fictitious set of system voltages, which gives the same average load power. The modified filter current algorithm gives correct compensation to obtain any desired source power factor for unbalance in source voltage magnitudes and/or phase angles. This can be called Equal Current Strategy, as the compensated three-phase source currents are balanced sinusoids. For the special case of unity power factor operation, an alternative Equal Resistance Algorithm has been also obtained. All these algorithms have been verified by simulation using MATLAB. The detailed simulation and experimental results have been given for each case with ideal inverter.

CHAPTER 3

DSTATCOM TOPOLOGIES FOR AC LOAD COMPENSATION

In the previous chapter the theories of shunt compensation were discussed. We have assumed that the shunt compensator that tracks the reference currents is represented by ideal current sources. In practice however these current sources are built around three-phase voltage source inverters (VSI). In three-phase distribution systems, a distribution static compensator (DSTATCOM) may have to inject a set of three unbalanced currents that may contain harmonics. The DSTATCOM must be able to inject currents in a phase independent of other two phases. Therefore, we need suitable topologies to realize the shunt algorithms. In this chapter, we concentrate on various topologies of shunt compensators. The merits and demerits of these topologies have been highlighted. The control aspect of DSTATCOM has been introduced and discussed. A neutral clamped DSTATCOM topology is chosen to realize a voltage source PWM inverter for ac load compensation. The simulation and experimental results are given for ac load compensation with this inverter circuit.

Active power filters are realized using various DSTATCOM topologies. A detailed literature survey on active power filters is given in [7]. Based on the topology, they are classified as shunt active, series active, series active and shunt passive (hybrid) and unified (shunt and series active) power filters. The compensator topologies may also be further classified based on the supply systems to which they are connected (e.g. single-phase two-wire, three-phase three-wire, three-phase four-wire supply systems) and the type of the converter used (e.g. voltage source inverter or current source inverter). Load configuration (i.e. star connected or delta connected) may also be used as criterion to distinguish three-phase active power filters.

In this chapter, we are mainly concerned with shunt compensators. Various shunt topologies for three phase distribution systems which may be three-phase, three-wire or three-phase, four-wire using VSI operating in current controlled mode are discussed. We shall start our discussion from generic single-phase DSTATCOM topologies. Based on the generic unit of compensation we evolve topologies for three-phase distribution systems.

3.1 DSTATCOM INVERTER TOPOLOGIES

First the current source inverter (CSI) DSTATCOM topology is described and its merits and demerits are given. Voltage source inverter (VSI) topology is discussed and compared with current source inverter topology. The soft switched and hard switched VSIs are also given. The generic hard switched VSI DSTATCOM topology for single phase is then extended for three phase DSTATCOM topology.

3.1.1 Current Source Inverter DSTATCOM Topology

A single phase and a three-phase version of current source inverter (CSI) topology are shown in Fig. 3.1 and 3.2 respectively [12-14]. Soft switching using Resonant LC circuit has also been applied to this configuration [72]. Current source uses inductive energy storage device i.e. inductor (L_f) in Fig. 3.1 and 3.2. The CSIs behave as nonsinusoidal PWM current source (i_f in Fig. 3.1 and i_{fa}, i_{fb}, i_{fc} in Fig. 3.2) to meet harmonic current requirement of the nonlinear load. In these figures a switch contains a switching devices (e.g. IGBT) and a diode in series. The series diode is used for reverse recovery blocking. However GTO based configurations do not use series diode, but they have restricted frequency of switching. These inverters are more reliable and fault tolerant than VSIs. They have disadvantages too as CSIs have higher losses, higher values of dc reactor and slow response. It is more difficult to use them in multi-level or multi-step mode to improve the performance in the higher power ratings.

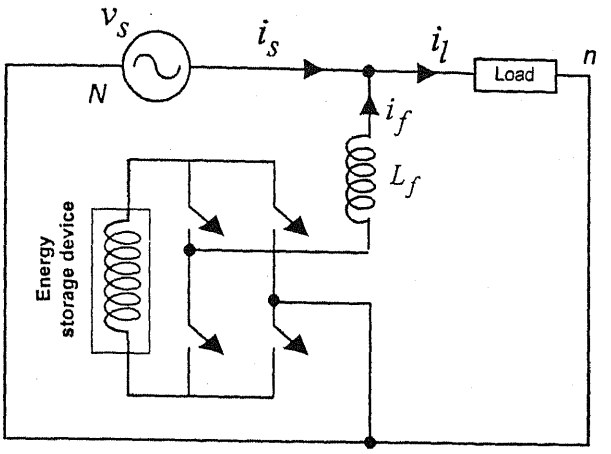


Fig. 3.1 Current source inverter DSTATCOM topology for single-phase distribution systems

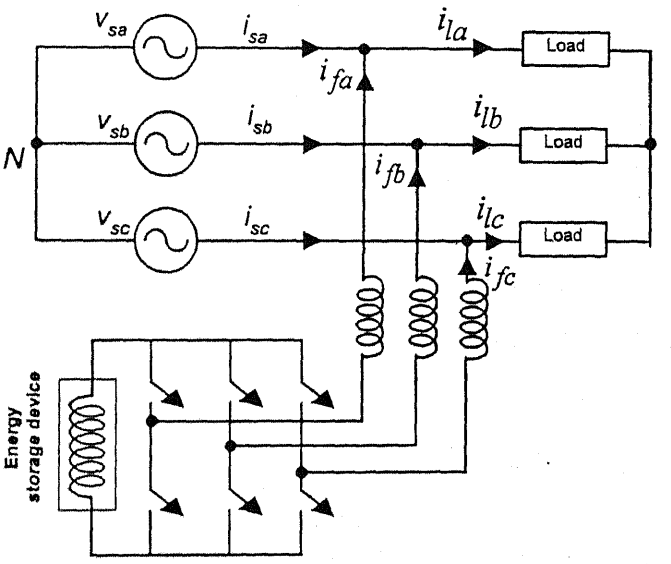


Fig. 3.2 Current source inverter DSTATCOM topology for three-phase distribution systems

3.1.2 Voltage Source Inverter DSTATCOM Topology

Voltage source inverter DSTATCOM topology uses dc capacitor as energy storage device. As regards to energy storage capacitive elements are far more efficient, smaller and less expensive than inductive ones. However, where very large amount of energy is required, super-conductive inductors can be used with CSIs [12]. There is another class of power circuit for the active power filters, namely active power filter with hybrid energy source

[15]. Hybrid structure includes both inductive and capacitive elements together. Through suitable logic, the two energy storage elements are interfaced. However the control is complex for such configurations.

Voltage source inverter (VSI) is however preferred over the current source inverter topology, because the voltage source inverter is higher in efficiency and lower in initial cost than the current source inverter. For the above reasons, VSIs are becoming more popular choice in realizing the compensator. Soft switched and hard switched VSI DSTATCOM are described in the following.

Soft Switched VSI DSTATCOM Topology

A single-phase soft switched inverter topology is given in Fig. 3.3. This topology may also be referred as Resonant DC Link Inverter (RDCLI) topology [73-74]. This inverter topology needs minimum number of devices. It is easy to implement and requires a simple control. Compared to a regular pulse width modulated (PWM) inverter, this inverter requires an additional resonant inductor and a resonant capacitor. The resonant circuit is connected between dc source and the inverter so that the input voltage to the inverter oscillates between zero and a value that is slightly greater than twice the dc bus voltage. The advantage of this soft-switched inverter is well known [73]. It reduces the dominant switching losses in the inverter devices, allows higher switching frequencies at reasonably high power level and reduces noise and electromagnetic interference. Because of the minimal switching loss, the efficiency is high and cooling requirement is minimal. Additionally, the devices do not require any snubber.

This topology contains a resonant circuit generated by an inductor (L) and a capacitor (C) as shown in this Fig. 3.3. The inductor coil has a resistance (R) due to its finite Q-factor. The voltage (v_C) across the capacitor is called the dc link voltage. Using the resonant circuit properties, this voltage goes through zero periodically. The switch (S_0) shown in Fig. 3.3 represents the switch across the link. This switch is required to short the link when the voltage v_C is zero for the current i_R to build up. The current i_{r0} is the input current of the inverter, which acts as the load current for the resonant link. Its three-phase version can

also be employed. Then the topology uses six switches (S_1-S_6) instead of the four switches shown in Fig. 3.3

This simple topology however has few drawbacks. These are higher device voltage stresses (when the output voltage is greater than twice the dc input voltage) and the zero crossing failure unless the initial current in the resonant inductor is built properly. Though RDCLI topology provides better bandwidth along with the other advantages, they are associated with utilization difficulties in three phase distribution systems and in multi-level inverters. Further the dynamic performance is poor. Due to the above reasons hard switched VSI DSTATCOM are preferred.

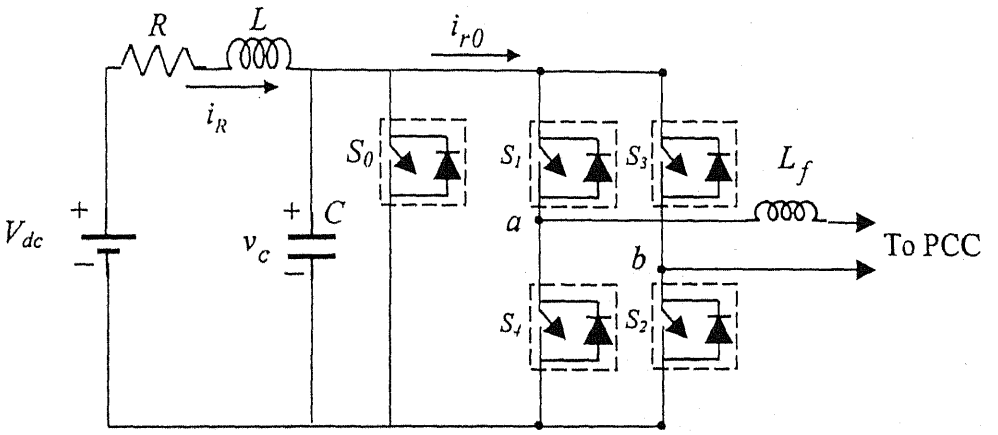


Fig. 3.3 Resonant dc link inverter for DSTATCOM

Hard Switched VSI DSTATCOM Topology

A typical single phase VSI DSTATCOM topology is shown in Fig. 3.4 [17, 19, 51, 75]. It consists of four switches (S_1-S_4) to realize a single-phase H-bridge inverter. In this figure each switch contains a switching device (e.g. IGBT) and an anti-parallel diode. Henceforth this will be the standard representation of a switch. The topology has one dc storage capacitor (C). It has an interfacing inductor L_f connected between middle point of the inverter leg and point of common coupling (PCC). At higher distribution voltage levels the use of an interface transformer is necessary. The primary of the transformer is connected between points a and b whereas the secondary is connected between PCC and neutral of the load. In this case the interfacing inductor includes the leakage inductance of the transformer. The topology has fast dynamic performance and is the most commonly used

DSTATCOM topology for load compensation. The corresponding three-phase DSTATCOM has several versions. These will be discussed in Section 3.2.

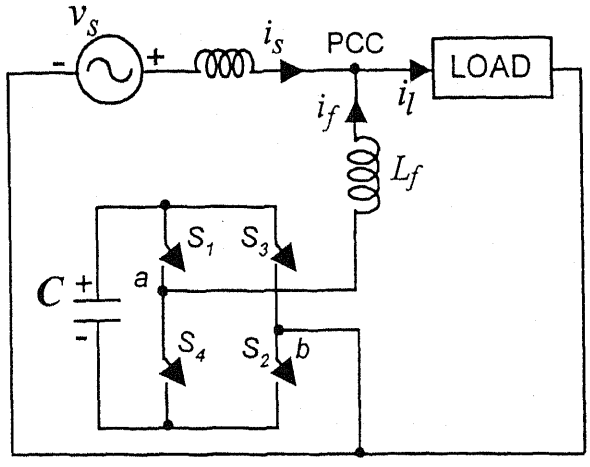


Fig. 3.4 Single phase VSI DSTATCOM topology

3.2 THREE-PHASE DSTATCOM TOPOLOGIES

One of the ways to realize a three-phase DSTATCOM topology is to use three independent single-phase units (Fig. 3.5), each with a voltage source inverter (VSI) along with a dc storage capacitor. Controlling the three capacitor voltages through control of one variable term P_{loss} (Equation 2.19 of Chapter 2) will be an impossible task [46].

In a practical inverter a voltage regulator loop is incorporated to regulate the voltage of each capacitor. Thus for three capacitors we need three such capacitor voltage control loops. The variation of voltage of each capacitor will depend upon the nature of reference currents and the load currents in the respective phases. Therefore each VSI will have a different loss in the circuit. Suppose there are three identical units of VSI each with equal value of the capacitor, C. Three independent PI regulators produce three terms P_{loss1}, P_{loss2}, and P_{loss3}. Each of these is used in the corresponding phase to modify $\bar{p}_l$ in (2.75). In (2.75) $\beta = 0$ for unity power factor operation and $\bar{p}_l$ is modified to $\bar{p}_l + P_{loss\,j}$, $j = 1$, 2, 3. The resulting capacitor voltages are shown in Fig. 3.6. Since in the steady state, the three terms P_{loss1}, P_{loss2}, and P_{loss3} are not equal so unequal powers are drawn from

source to balance the voltage of the capacitors. As a result of which the source currents (hysteresis band of 1 A) become unbalanced as shown in Fig. 3.7. Thus the purpose of shunt compensation is completely lost. Therefore we conclude that the use of three VSIs with three capacitors is not justified as it is neither economical nor does it result in satisfactory operation.

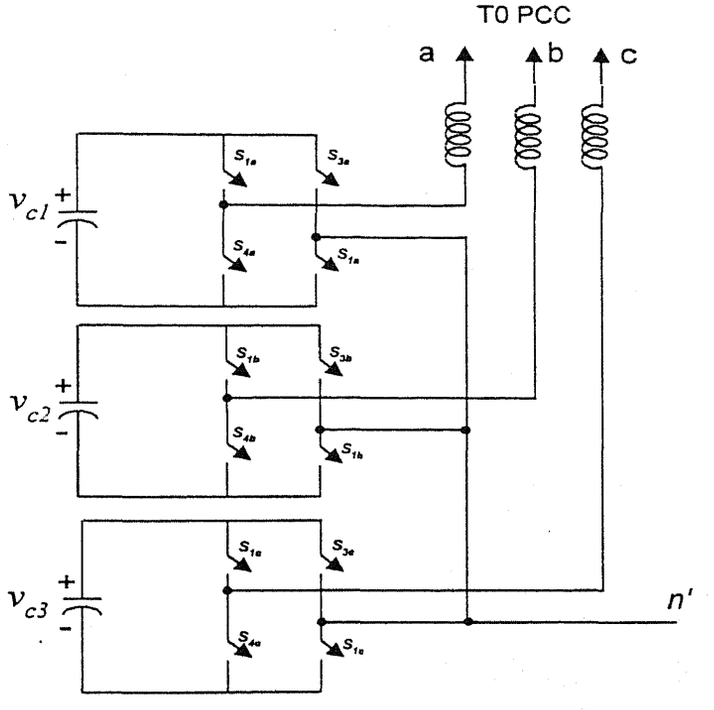


Fig. 3.5 Three-phase, three-leg topology with 3 dc storage capacitors

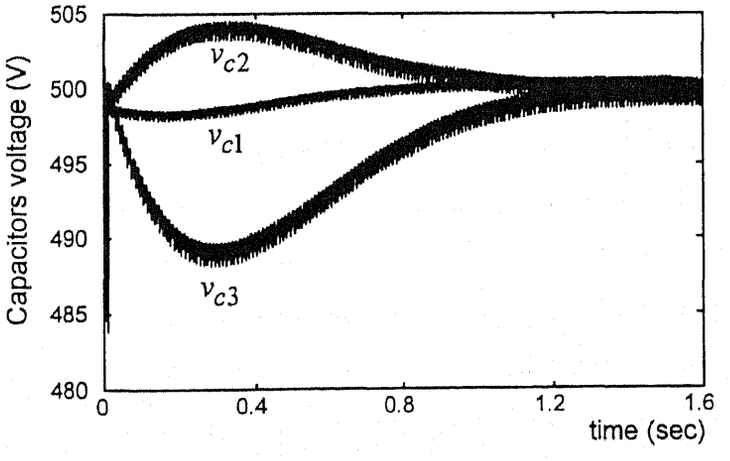


Fig. 3.6 Capacitors voltage with three single phase VSI

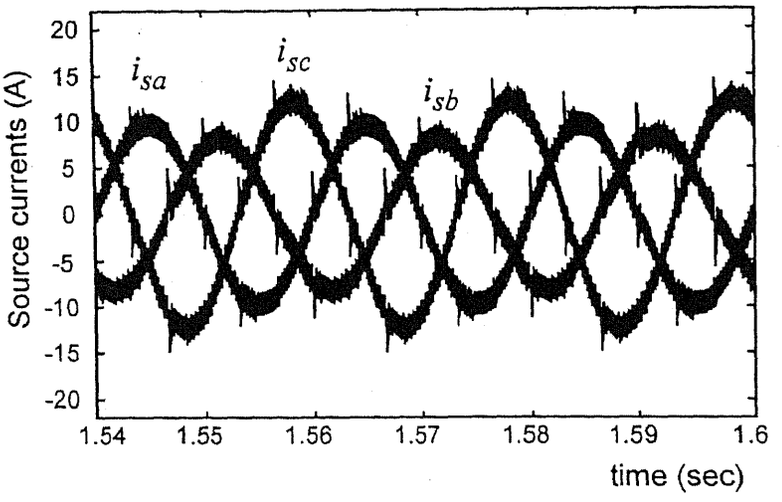


Fig. 3.7 Unbalanced source current

The solution to this problem is to use one dc capacitor instead of three. This topology is discussed in the next section.

3.3 THREE INDEPENDENT SINGLE PHASE INVERTERS WITH SINGLE DC STORAGE CAPACITOR

A typical DSTATCOM structure is shown in Fig. 3.8. It contains three H-bridge VSIs that are connected to a common dc storage capacitor. Each VSI is connected to the network through a transformer. Six output terminals of the transformer are connected in star. These six terminals can also be connected in delta to compensate a Δ-connected load. In this case, each transformer is connected in parallel with the corresponding load [37, 46]. The purpose of including the transformers is to provide isolation between the inverter legs. This prevents the dc storage capacitor from being shorted through switches in different inverters as shown in Fig. 3.9. The power switches S_{1a}-S_{2a} *and* S_{3a}-S_{4a} in VSI of phase-*a* are operating in complimentary mode, i.e. if S_{1a} and S_{2a} are ON, *then* S_{3a} and S_{4a} are OFF and vice versa. This is also true for power switches of VSI in phases *b* and *c*. It is to be noted that this circuit will short the capacitor if interface inductors are directly connected to the PCC instead of transformers. The transformers also provide voltage level conversion if required.

The inductance L_f in this Fig. 3.8 represents the leakage inductance of each transformer and additional external inductance, if any. The switching losses of an inverter and the copper losses of the connecting transformer are represented by a resistance R_f. The iron losses of the transformer are neglected. For a star connected load, the neutral point of the three transformers is connected to the load neutral.

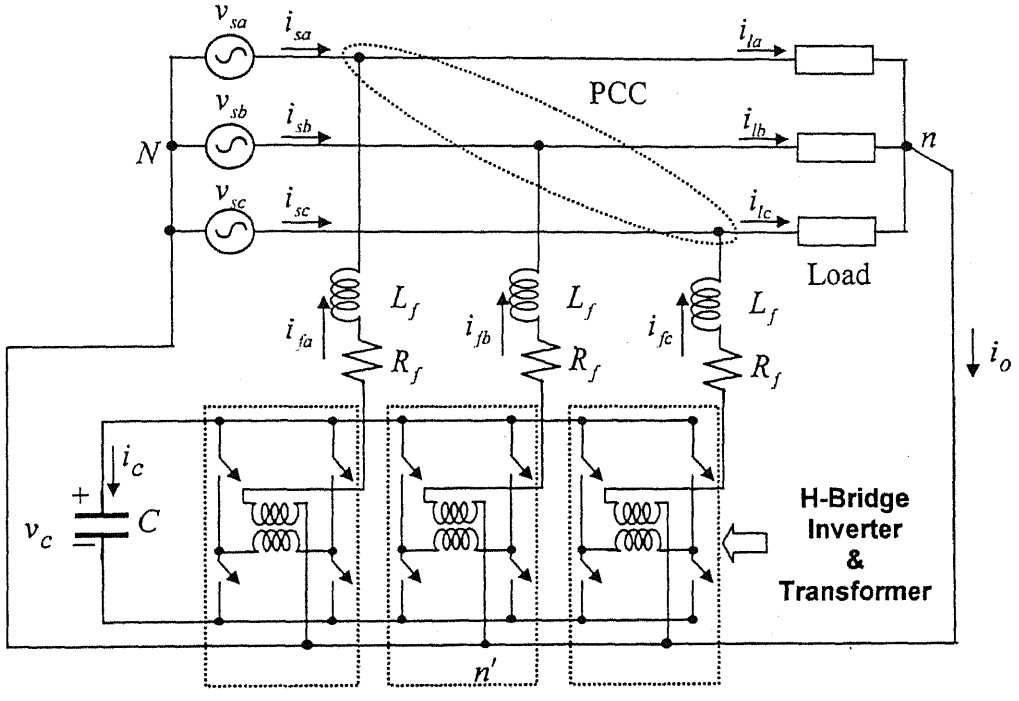


Fig. 3.8 A compensator topology with three independent, single-phase VSI supplied from a common dc storage capacitor

The topology however is not suitable for compensation of loads containing dc components in addition to ac components in the load current. The presence of isolation transformers does not allow the dc component of the load current to be compensated. This current therefore returns to the system neutral and results in the poor quality of source currents.

It is to be noted that presence of dc component in the load current is not very uncommon. Consider a situation in industries with number of machines connected to supply systems. The loads may contain several large and small rating three-phase, single-phase half-wave rectifiers, which contribute to the dc component. Not only that, some dc

component may even be present in the ac system. However its presence may not be felt due to sturdy ac system. Hence a compensator topology suitable for compensating dc load is also required. This is described in Chapter 4.

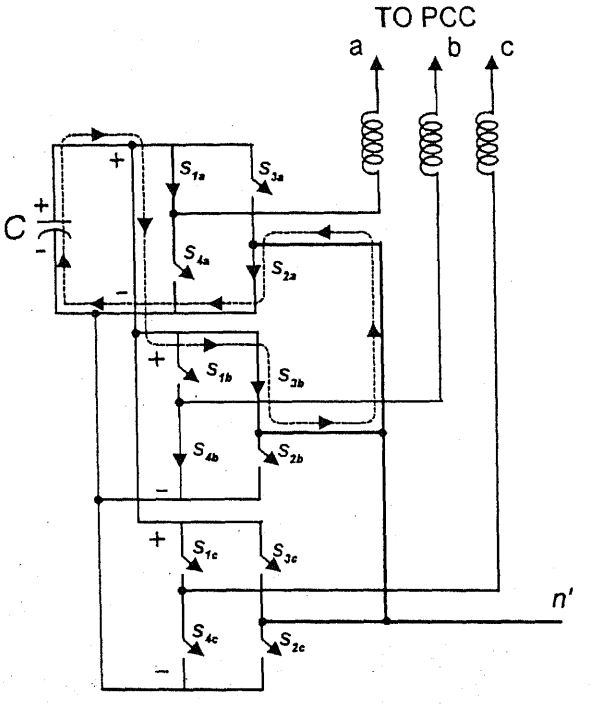


Fig. 3.9 Shorting of dc capacitor without isolation transformer

3.4 A THREE-PHASE, THREE-LEG TOPOLOGY

A three-phase, three-leg topology is shown in Fig. 3.10. If we use three-phase, single dc storage capacitor topology, then load with zero sequence currents can not be compensated and the zero sequence current flows in the neutral wire (*N-n*). The zero sequence thus returns to the ac distributions system and it also enters the ac system, thus degrading the quality of source currents. If the load is nonlinear and contains harmonics, then these harmonics also enter to the ac system and thus degrading the power quality. In this topology the generation of the three compensator currents is not independent i.e. $i_{fa} + i_{fb} + i_{fc} = 0$. Hence this scheme is not suitable three-phase, four-wire distribution systems with loads containing zero sequence currents.

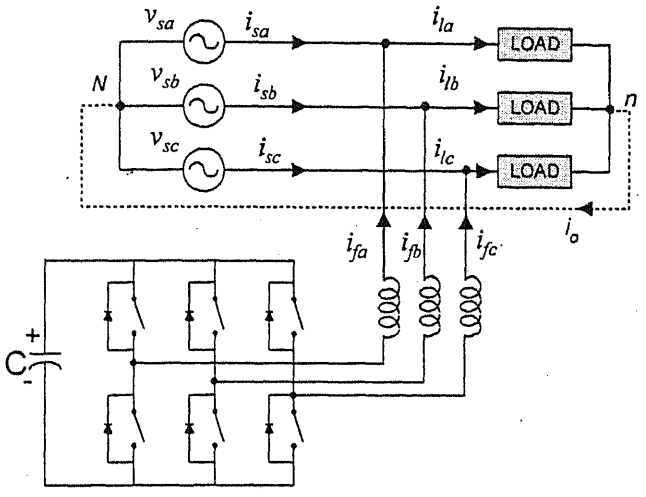


Fig. 3.10 A three-phase, three-leg DSTATCOM topology

To overcome the aforesaid problems, a three-phase, four-leg topology is suggested. This topology is discussed in the next section.

3.5 THREE PHASE FOUR LEG TOPOLOGY

The three-phase, four-leg inverter topology shown in Fig. 3.11 and is suitable for the dc elimination of zero sequence from the source current if the load current contains dc components [39, 72]. It has a VSI with four legs and one dc storage capacitor. Three of its legs are used for phase connection while the fourth leg is connected to the load neutral and supply neutral, if available, through a reactance.

The reference current for the fourth leg is the negative sum of three phase load currents. This nullifies the effect of dc component of load current. To maintain the adequate charge on dc-side capacitor a PI regulator is used to control the flow of real power from ac side towards dc side of the converter.

When the compensator is working, zero sequence current is routed to path $n-n'$ containing switching frequency harmonics. Using fourth leg of inverter, the negative of zero sequence current $-i_o$ is tracked. Certainly it needs a higher bandwidth VSI to track

negative of neutral current ($-i_o$) as i_o contains harmonics due to non-linear loads. This increases the switching losses. If this current is not tracked properly, it will leave high switching frequency current components in the *N-n* path, which is not desirable. To overcome the above problems a new DSTATCOM topology is proposed in the next chapter.

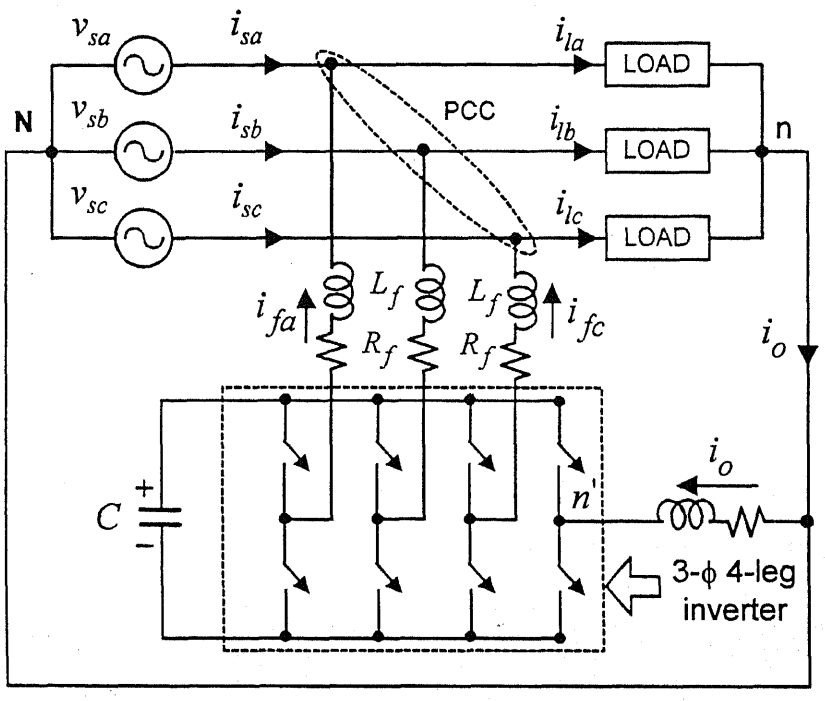


Fig. 3.11 A compensator structure which uses a four-leg VSI

3.6 NEUTRAL CLAMPED INVERTER TOPOLOGY

The neutral clamped inverter topology is shown in Fig. 3.12 [20, 38, 55, 75-77]. The topology consists of two dc storage capacitors (C_1, C_2) of same rating and a three-phase VSI. Each leg of the inverter has two IGBT switches with anti parallel diodes across them. In this circuit the junction (n') of the two capacitors is connected to the neutral of the load. This neutral clamped topology allows a path for the zero-sequence current and therefore the three injected currents can be independently controlled. Note that in Fig. 3.12 there is no isolation transformer and each leg of the VSI is connected to the point of common coupling

3.7 GENERATION OF REFEENCE CURRENTS WITH INVERTER CIRCUIT

In this Section, we consider the circuit of Fig. 3.12 operating under the general algorithm (2.68). In an actual compensator, the inverter has finite bandwidth and also has some losses. Therefore the source should supply not only the power to load but also the inverter losses keeping the total capacitor voltage ($v_c = v_{c1} + v_{c2}$) to a reference value ($2V_{c\,ref}$). The reference currents for Case 2 in Table 2.1 are obtained by modifying (2.68) as follows,

$$\left.\begin{aligned} i^*_{fa} &= i_{la} - \frac{v_{sa} + \gamma\left(v_{sb} - v_{sc}\right)}{\sum_{i=a,b,c} v_{si}^2}\left(\bar{p}_l + P_{loss}\right) \\ i^*_{fb} &= i_{lb} - \frac{v_{sb} + \gamma\left(v_{sc} - v_{sa}\right)}{\sum_{i=a,b,c} v_{si}^2}\left(\bar{p}_l + P_{loss}\right) \\ i^*_{fc} &= i_{lc} - \frac{v_{sc} + \gamma\left(v_{sa} - v_{sc}\right)}{\sum_{i=a,b,c} v_{si}^2}\left(\bar{p}_l + P_{loss}\right) \end{aligned}\right\} \tag{3.1}$$

where $\gamma = \tan\phi/\sqrt{3}$, ϕ is the desired phase angle between supply voltages v_{sa}, v_{sb} and v_{sc} and line currents i_{sa}, i_{sb} and i_{sc} respectively. Note that for unity power factor operation $\phi = 0$ and therefore $\gamma = 0$. Therefore reference compensator currents for unity power factor of the source, become

$$\left.\begin{aligned} i_{fa}^{*} &= i_{la} - \frac{v_{sa}}{\sum_{i=a,b,c} v_{si}^{2}}\left(\bar{p}_l + P_{loss}\right) \\ i_{fb}^{*} &= i_{lb} - \frac{v_{sb}}{\sum_{i=a,b,c} v_{si}^{2}}\left(\bar{p}_l + P_{loss}\right) \\ i_{fc}^{*} &= i_{lc} - \frac{v_{sc}}{\sum_{i=a,b,c} v_{si}^{2}}\left(\bar{p}_l + P_{loss}\right) \end{aligned}\right\} \tag{3.2}$$

The term $\bar{p}_l$ is the average value of the load power and is computed using a moving average filter (MAF) that has an averaging time of half a cycle. The term P_{loss} in (3.1) and (3.2) accounts for the losses in the inverter.

To generate P_{loss} a suitable feedback controller is used, that regulates the sum of dc capacitors voltage to a pre-defined value. The objective here is to hold the capacitor total voltage i.e. $(v_{c1} + v_{c2})$ to a constant equal to $2V_{cref}$, where V_{cref} is the reference voltage of each capacitor. We have $v_{c1} = \frac{1}{C_1}\int i_1 dt$ and $v_{c2} = \frac{1}{C_2}\int i_2 dt$. The currents i_1 and i_2 are inverter input currents as shown in Fig. 3.12. Therefore any deviation of $v_c = v_{c1} + v_{c2}$ from $2V_{cref}$ gives a good indication of the deviation of the average value of the capacitor current from zero. We thus choose a simple proportional plus integral (PI) controller of the form

$$P_{loss} = K_p\, e_c + K_i \int e_c\, dt \tag{3.3}$$

$$e_c = e_{c1} + e_{c2} = 2V_{cref} - \left(v_{c1} + v_{c2}\right) \tag{3.4}$$

where,

$$e_{c1} = V_{cref} - v_{c1}, \quad e_{c2} = V_{cref} - v_{c2} \tag{3.5}$$

The control scheme for VSI as current source is shown in Fig 3.13.

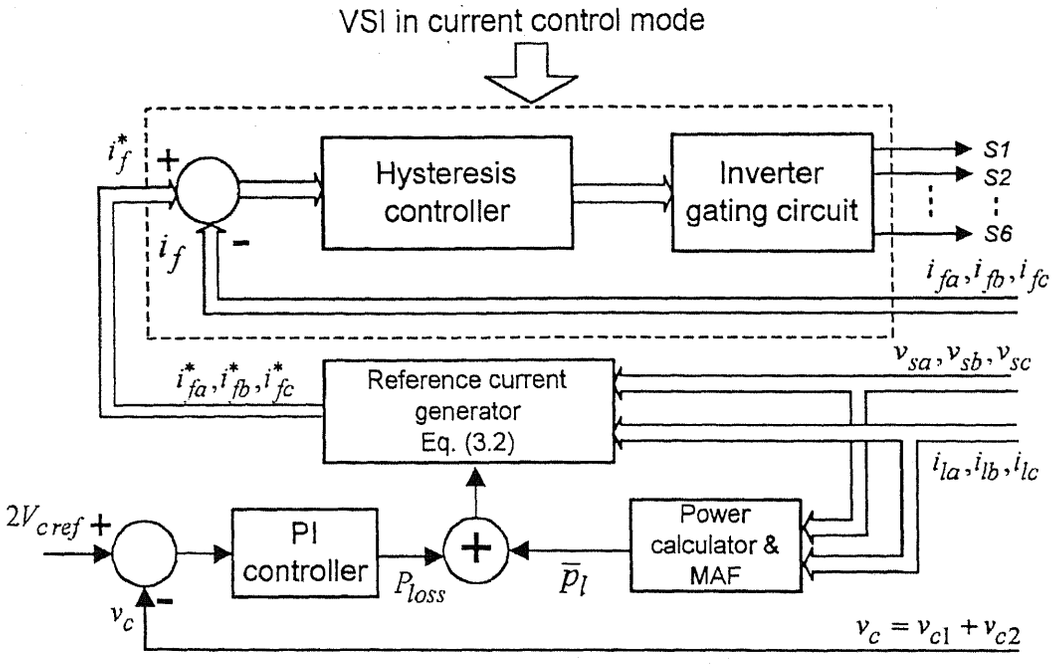


Fig. 3.13 Control scheme for VSI operating as current source

3.8. STATE SPACE MODEL FOR COMPENSATOR

Let the gating signal for switch S_1 in Fig. 3.12 is represented by a binary variable S_a. If $S_a = 1$, S_1 is closed, and if $S_a = 0$, S_1 is open. A gating signal for S_4 is the complementary signal $\bar{S}_a$. Similarly S_b, $\bar{S}_b$, S_c, $\bar{S}_c$ represent gating signals for switches S_3, S_6, S_5, S_2 respectively. The switches of the inverter ($S_1 - S_6$) are operated such that one switch in each leg is always gated. Therefore the current i_1 and i_2 in the input lines of the inverter (Fig. 3.12) can be written in terms of inverter currents and gating signals as follows.

$$i_1 = S_a\, i_{fa} + S_b\, i_{fb} + S_c\, i_{fc} \tag{3.6}$$

$$i_2 = \bar{S}_a\, i_{fa} + \bar{S}_b\, i_{fb} + \bar{S}_c\, i_{fc} \tag{3.7}$$

The switches S_1 to S_6 are operated in the hysteresis current control mode (Fig. 3.13). When the current i_{fa} hits a pre-calculated lower limit, switch S_1 is closed. The equivalent circuit for this mode is shown in Fig 3.14. The load of phase-a is not shown as it is in parallel with v_{sa} and does not appear in the equations of the model.

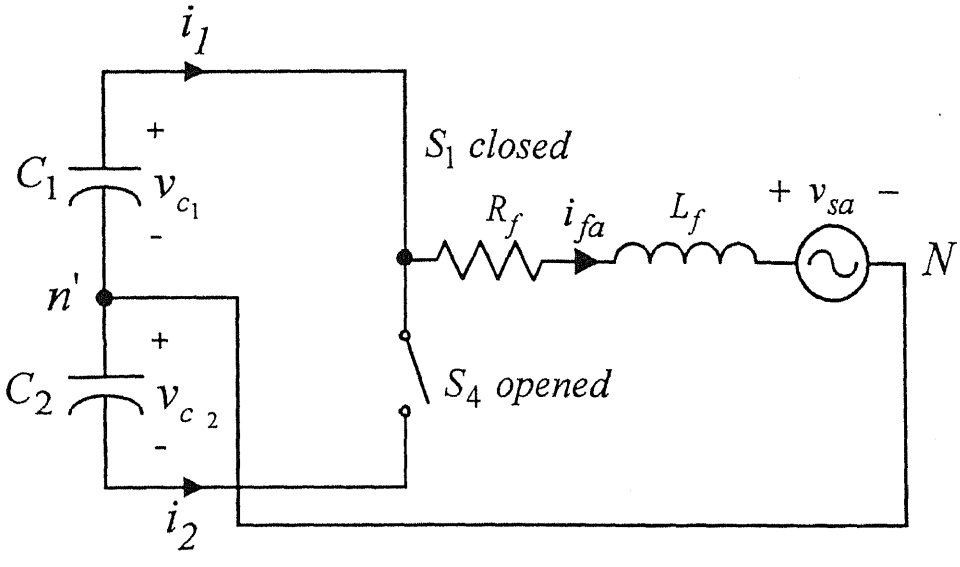


Fig. 3.14 Equivalent circuit for phase a when S_1 is on and S_4 is off

Applying KVL around the loop we get

$$\frac{di_{fa}}{dt} = -\frac{R_f}{L_f} i_{fa} + \frac{v_{c_1}}{L_f} - \frac{v_{sa}}{L_f} \tag{3.8}$$

Similarly if the current i_{fa} hits a pre-calculated upper limit, switch S_1 is opened and S_4 is closed. From an equivalent circuit similar to Fig. 3.14, we can write,

$$\frac{di_{fa}}{dt} = -\frac{R_f}{L_f} i_{fa} - \frac{v_{c_2}}{L_f} - \frac{v_{sa}}{L_f} \tag{3.9}$$

Using the binary variables S_a and $\bar{S}_a$ defined above we get from (3.7)-(3.8)

$$\frac{di_{fa}}{dt} = -\frac{R_f}{L_f} i_{fa} + S_a \frac{v_{c_1}}{L_f} - \bar{S}_a \frac{v_{c_2}}{L_f} - \frac{v_{sa}}{L_f} \tag{3.10}$$

Similarly for phases b and c, we have,

$$\frac{di_{fb}}{dt} = -\frac{R_f}{L_f} i_{fb} + S_b \frac{v_{c_1}}{L_f} - \bar{S}_b \frac{v_{c_2}}{L_f} - \frac{v_{sb}}{L_f} \tag{3.11}$$

$$\frac{di_{fc}}{dt} = -\frac{R_f}{L_f} i_{fc} + S_c \frac{v_{c_1}}{L_f} - \bar{S}_c \frac{v_{c_2}}{L_f} - \frac{v_{sc}}{L_f} \tag{3.12}$$

Equating currents in capacitor C_1 to $-i_1$ and in C_2 to i_2 and using (3.6)-(3.7), we get,

$$\frac{dv_{c1}}{dt} = -S_a \frac{i_{fa}}{C} - S_b \frac{i_{fb}}{C} - S_c \frac{i_{fc}}{C} \tag{3.13}$$

$$\frac{dv_{c2}}{dt} = \bar{S}_a \frac{i_{fa}}{C} + \bar{S}_b \frac{i_{fb}}{C} + \bar{S}_c \frac{i_{fc}}{C} \tag{3.14}$$

where $C_1 = C_2 = C$.

Through (3.10)-(3.14), we obtain the following state space model

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\,\boldsymbol{x} + \boldsymbol{B}\,\boldsymbol{u} \tag{3.15}$$

where,

$$\boldsymbol{x} = [i_{fa} \quad i_{fb} \quad i_{fc} \quad v_{c1} \quad v_{c2}]^t \,,\ \boldsymbol{u} = [v_{sa} \quad v_{sb} \quad v_{sc}]^t$$

where,

$$\boldsymbol{A} = \begin{bmatrix} -R_f/L_f & 0 & 0 & S_a/L_f & -\bar{S}_a/L_f \\ 0 & -R_f/L_f & 0 & S_b/L_f & -\bar{S}_b/L_f \\ 0 & 0 & -R_f/L_f & S_c/L_f & -\bar{S}_c/L_f \\ -S_a/C & -S_b/C & -S_c/C & 0 & 0 \\ \bar{S}_a/C & \bar{S}_b/C & \bar{S}_c/C & 0 & 0 \end{bmatrix}$$

$$\boldsymbol{B} = \begin{bmatrix} -1/L_f & 0 & 0 \\ 0 & -1/L_f & 0 \\ 0 & 0 & -1/L_f \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

3.9. SIMULATION RESULTS

In this section we will demonstrate the feasibility of algorithm (3.2) with inverter circuit. The neutral clamped topology in Fig. 3.12 is chosen to verify the general algorithm proposed for shunt compensation in Chapter 2. For unity power factor operation with real inverter circuit, the expressions for reference currents are as given in (3.2). The system parameters are as same as considered in Section 2.7.2. These are also given in Table 3.1, in addition to the inverter parametres and PI controller gains.

Table 3.1 System parameters

System Parameters	Values
System frequency	50 Hz
Source voltages	100 V (peak)
Load	◆ $Z_a = 53\angle 22^o\,\Omega,\ Z_b = 96\angle 0^o\,\Omega,\ Z_c = 182\angle 28^o\,\Omega$ ◆ Three-phase full bridge diode rectifier drawing dc load current of 0.625 A
DC capacitors	$C_1 = C_2 = 2200\,\mu F$
Interface inductor	$R_f = 2\,\Omega,\ L_f = 40\,\text{mH}$
PI controller gains	$K_p = 10, K_i = 1$
Reference voltage	$V_{cref} = 130$ V
Hysteresis band	± 0.2 A

For the given system voltages and load configuration, the steady state load currents (i_{la}, i_{lb}, i_{lc}) and load powers (p_l, q_l) have been computed and shown in Fig. 2.9 (a) and (b) respectively. Using the samples of p_l, we compute average power ($\bar{p}_l$) using Moving Average Filter over half a cycle [46]. The dynamics of the compensator is modeled by solving the state space model discussed in Section 3.8. The switching of the inverter is done by monitoring the reference and the actual compensator currents and by comparison of the error in hysteresis band.

3.9.1 Steady State Performance

The source currents after compensation are shown in Fig. 3.15 (a). The source voltage in phase-*a* has also been shown to point out the unity power factor relation with source current in the same phase. The voltage is scaled to a factor of 32 in order to fit in the same graph. It is seen from the figure the source currents are balanced and sinusoidal but contain the high switching frequency of the inverter. The small notches are seen in source currents due to finite inductance of the interface inductor and discontinuities in load current. The neutral current is shown in Fig. 3.15 (b). The compensator is switched on after one cycle. After compensation, neutral current reduces to small value. However it possesses inverter switching frequency components. The spectrums of load and source currents are shown in Fig. 3.16 (a)-(f). The THD in load currents are 7.8%, 11.3%, 16.3% in phases a, b and c respectively. The spectrums of these currents are plotted in Fig. 3.16 (a), (c), (e) respectively. The THD in source currents after compensation are 3.92%, 2.68% and 2.89% in phases *a*, *b* and *c* respectively. The spectrums of source currents are plotted in Fig. 3.16 (b), (d), and (f) respectively. The THD is not equal in different phases of the source current. However, the reduction in the harmonic components is evident.

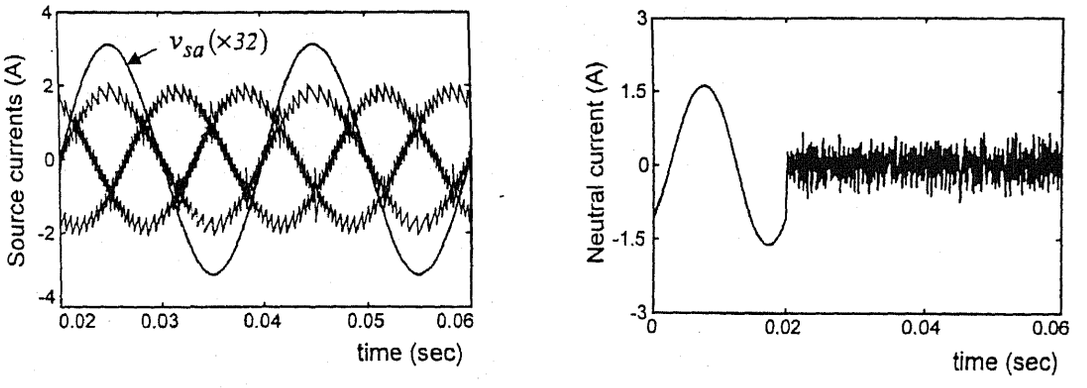


Fig. 3.15 (a) Source currents after compensation (b) Neutral current before and after compensation

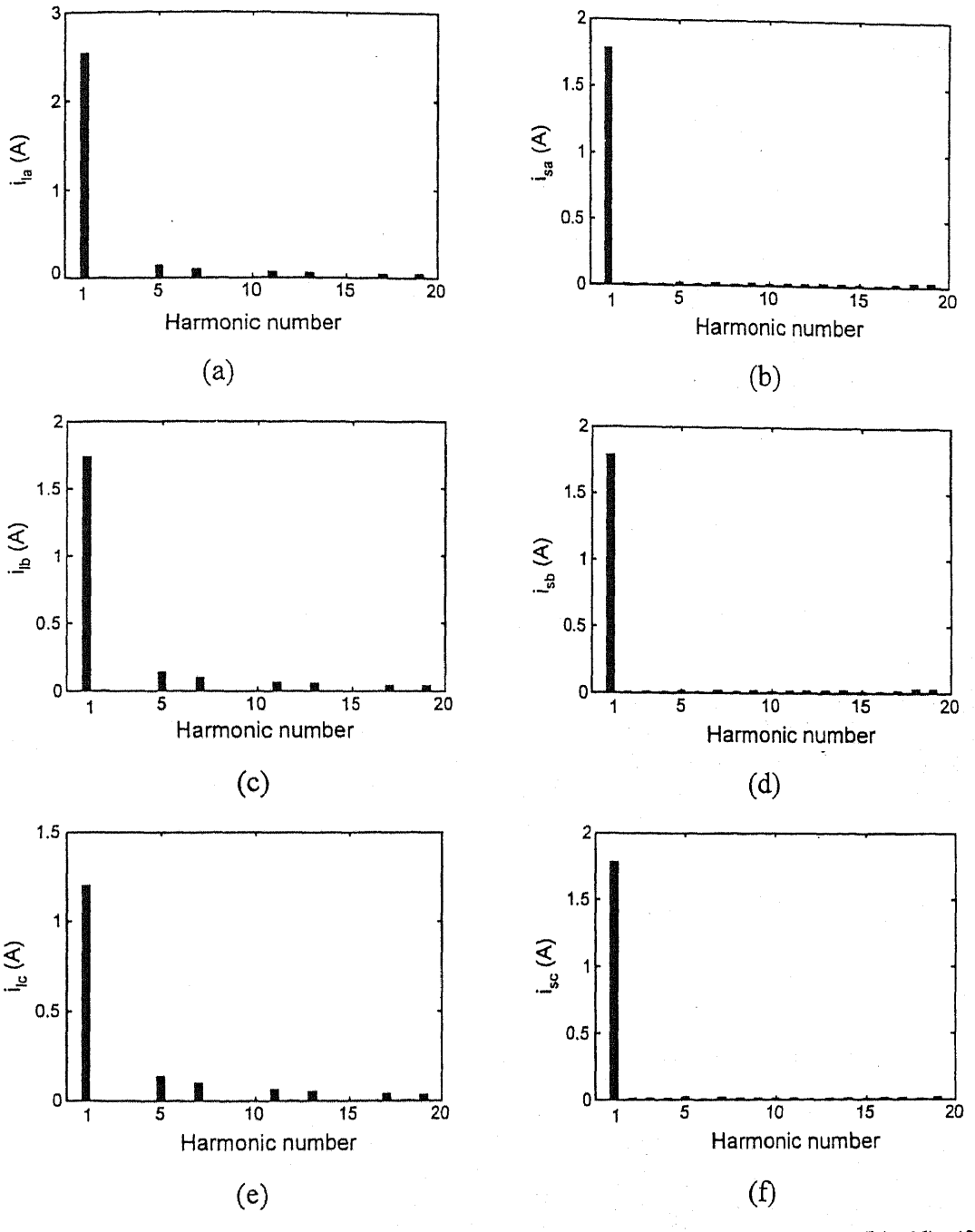


Fig. 3.16 Frequency spectrums of load currents(a), (c), (e) and source currents (b), (d), (f) in phases *a*, *b*, *c* respectively

The PI voltage regulator maintains total voltage (v_c) of dc capacitors nearly equal to $2V_{cref} = 260$ V. The voltage of the two capacitors are shown in Fig. 3.17. Voltage ripples are seen in these voltages as neutral current finds its path through these capacitors. The

compensator reference and actual currents in three phases are shown in Fig. 3.18 (a), (b) and (c) respectively. The source and compensator powers are shown in Fig. 3.19 and 3.20 respectively.

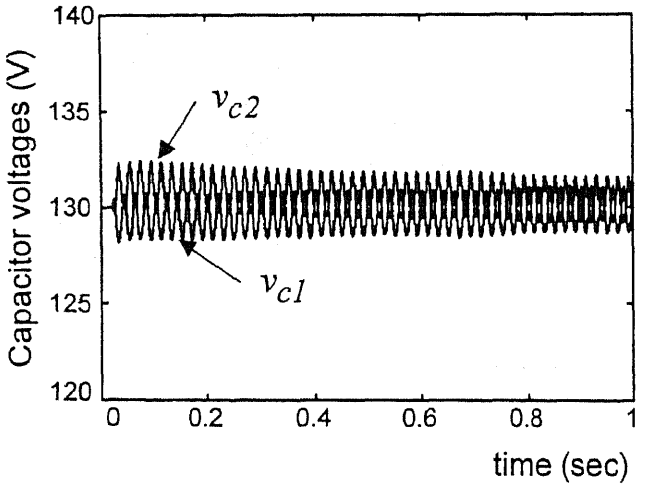


Fig. 3.17 Steady state dc capacitor voltages

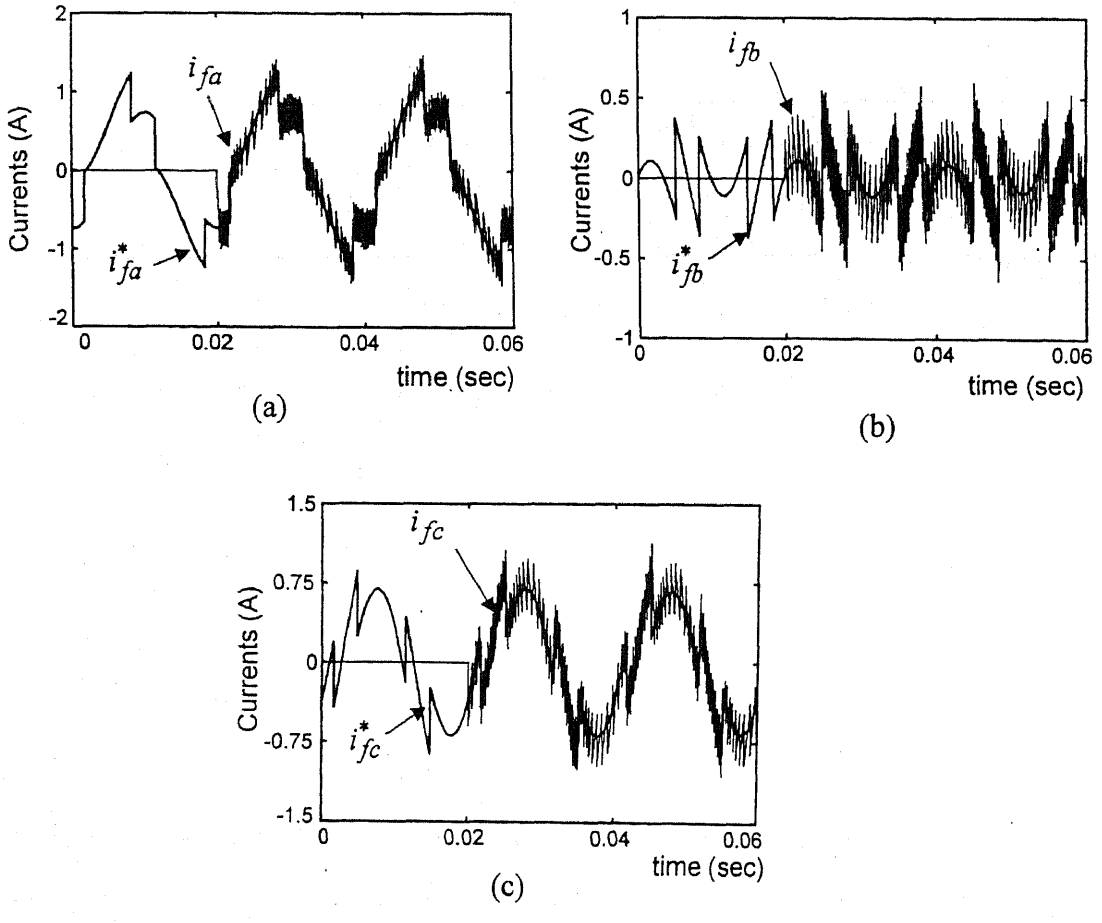


Fig. 3.18 Reference and actual compensator currents in (a) Phase-*a* (b) Phase-*b* (c) Phase-*c*

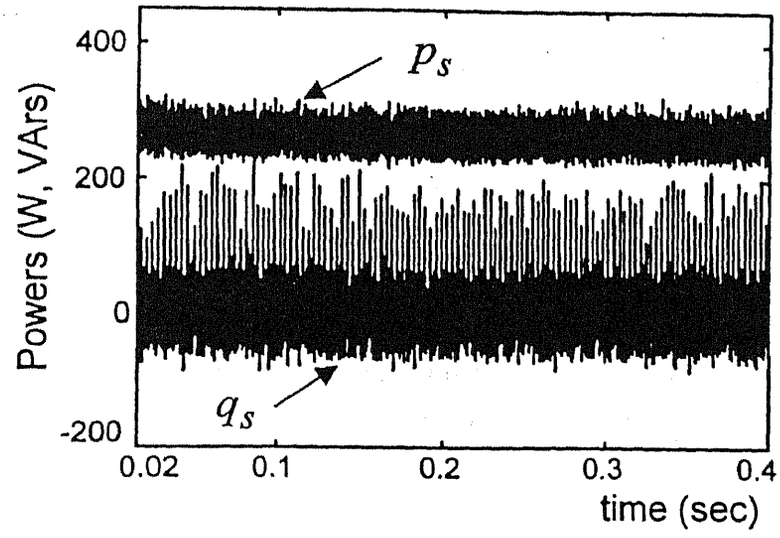


Fig. 3.19 Source active and reactive powers after compensation

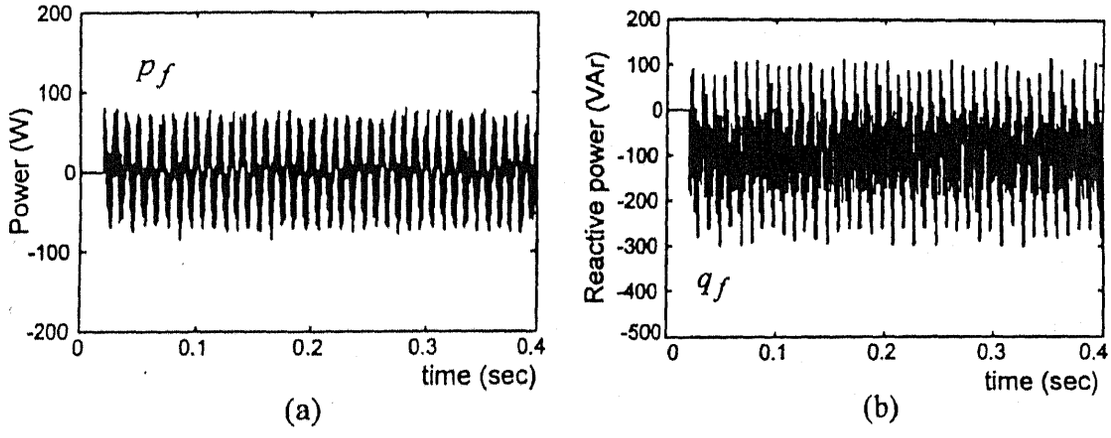


Fig. 3.20 Compensator powers (a) Active power (b) Reactive power

3.9.2. Transient Performance

The transient performance of the compensator is studied by changing the load. The R-L loads in phases *a* and *b* are changed as follows.

Region 1: The load is same as given in Table 3.1. The load in each phase is the sum of current due to R-L load and rectifier load in the respective phases.

Region 2: R-L loads in phases a and b are thrown off between 4^{th} and 10^{th} cycles (i.e. between $t = 0.08$ sec and $t = 0.2$ sec). Thus only rectifier load is present in phases a and b.

Region 3: The R-L loads in phases a and b are again switched on in the beginning of 11^{th} cycle, i.e. $t = 0.2$ sec. The rectifier load is retained in each phase.

These three regions are indicated above and the load currents are shown in Fig. 3.21 (a). The load in phase-c is unchanged throughout this period. It is seen from the Fig. 3.21 (b) that when loads in phases a and b are thrown off (a transition from Region 1 to Region 2), there is a rise in v_c. This is because, as load is thrown off, there is a surplus of power drawn from the source and it raises the voltage v_c transiently. The PI control action brings v_c back to $2V_{cref}$ within few cycles in the Region 2. At the end of 10^{th} cycle (Beginning of Region 3), loads in phases a and b are reconnected. At this time ($t = 0.2$ sec), there is a voltage dip in v_c as there is a sudden increase in load power and it is transiently supplied by the dc capacitors. Again after few cycles v_c settles around $2V_{cref}$ as a result of PI control action. Thus, dc capacitors act as energy reservoir under transient load conditions.

The variation of P_{loss} is shown in Fig. 3.21 (c). There is a dip in P_{loss} when load is thrown off as v_c rises above $2V_{cref}$. It is clearly seen from Fig. 3.21 (c) when the load is reconnected at $t = 0.2$ sec, there is a rise in P_{loss} because v_c is reduced below $2V_{cref}$. The source currents in phases a, b and c during the load transient are shown in Fig. 3.21 (d), (e) and (f) respectively. It can be seen from Fig. 3.21 (d)-(f) that the source currents in three phase are balanced and sinusoidal. The source currents settle within one cycle for transient on the load side. Thus the compensator exihibts fast response due to moving average filter used in the computation of average load power in the load ($\bar{p}_l$). The average load power may also be obtained by using a Butterworth low-pass filter as suggested in [78]. However settling time involved in this is fairly larger.

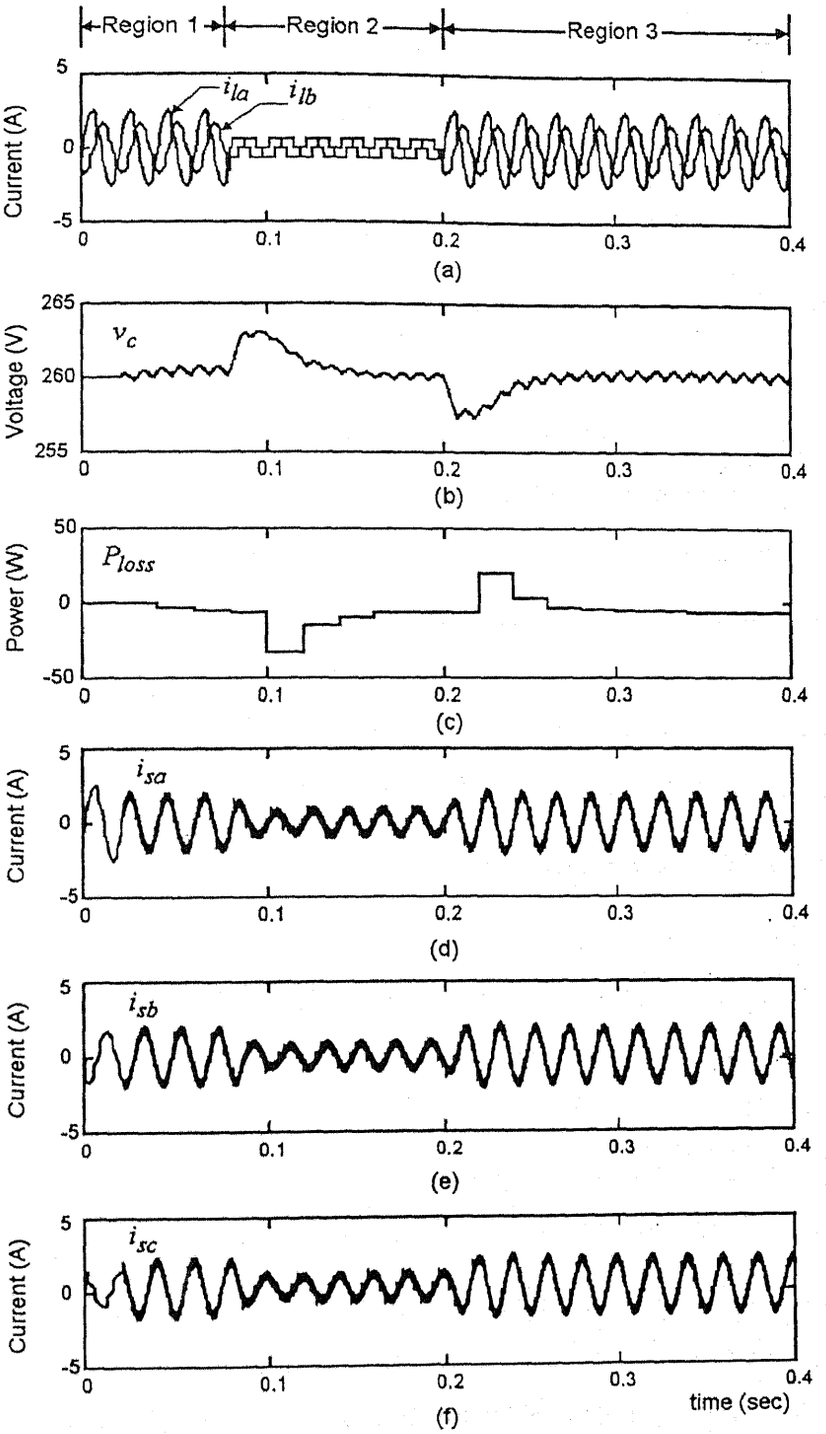


Fig. 3.21 (a) Load currents in phases *a* and *b* (b) Total dc capacitor voltage (c) Variation of P_{loss}, Source current in (d) Phase-*a* (e) Phase-*b* and (f) Phase-*c*

3.10 EXPERIMENTAL RESULTS

In this section experimental results are presented with inverter circuit. The source voltages are balanced and sinusoidal with a peak of 100 V volts. The system parameters are approximately same as given Table 3.1. The PI controller gains in capacitor voltage regulator loop are $K_p = 30$ and $K_i = 6$. Each dc capacitor is regulated to 130 V.

The system voltages v_{sa}, v_{sb}, v_{sc} and load current i_{la}, i_{lb}, i_{lc} are sensed using Hall effect voltage and current transducers The positions of theses transducers are shown in Fig. A.1 in Appendix A. The voltage and current signals are acquired by PC (P-II, 350 MHz) through data acquisition card (9118 DG NuDAQ). The algorithm for reference filter currents is implemented in Turbo C language. To obtain the average load power ($\bar{p}_l$), moving average filter has been implemented in the software. Then, filter reference currents are generated using (3.2). This computation takes about 35 μ sec. This speed is sufficient to generate filter currents containing harmonics up to 3 kHz, through a VSI based current source using hysteresis control provided the VSI has sufficient bandwidth.

3.10.1 Steady State Performance

The steady state load currents and load powers are shown in Fig. 3.22 and 3.23 respectively. Due to unbalanced R-L load and diode rectifier load, the load currents are unbalanced and exhibit abrupt changes. These load currents result in active and reactive load power as shown in Fig. 3.23. From 3.23, average load power is ($\bar{p}_l$) is approximately 250 W while average reactive load power is approximately –60 VAr. The waveforms of load currents and load powers are similar to that shown in Fig. 2.9 (a) and (b) respectively.

The neutral current before and after compensation are shown in Fig. 3.24. It is seen that after compensation the neutral current reduces considerably. The compensated source currents are shown in Fig. 3.25. The source currents are balanced and sinusoidal. They are also in phase with the source voltages. Howevwer they contain inverter switching frequencies. Unity power factor relationship between source currents and voltages is shown in Fig. 3.26. The frequency spectrum of source current in phase-*a* is shown in Fig. 3.27, which compares well with Fig. 3.16 (b) obtained by simulation. The THD of source current

is 3.92%, which is below 5% specified by IEEE-519 standard. The THD for source currents in other phases has a similar figure. The THD for experimental load currents is nearly same as for simulated load currents as discussed in Sub-section 3.9.1.

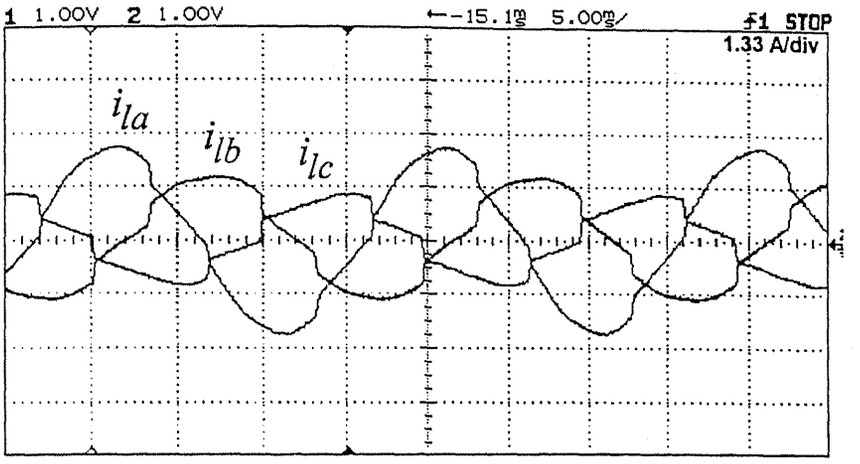


Fig. 3.22 Experimental load currents

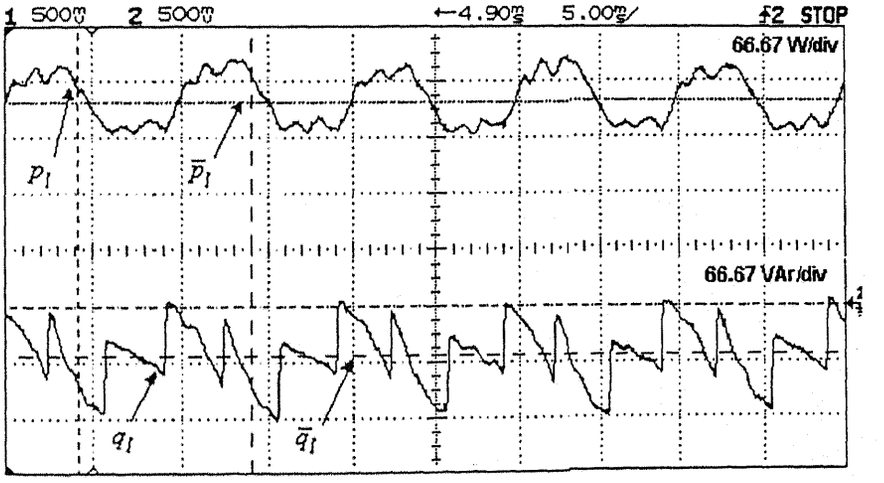


Fig. 3.23 Active and reactive load powers

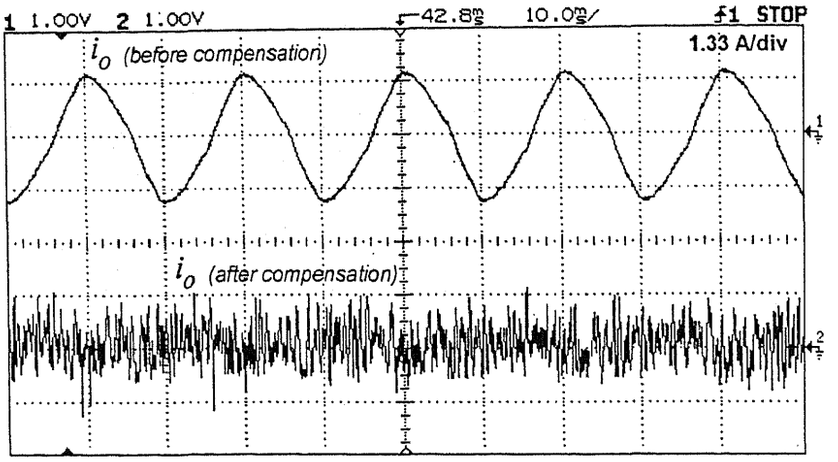


Fig. 3.24 Neutral current before and after compensation

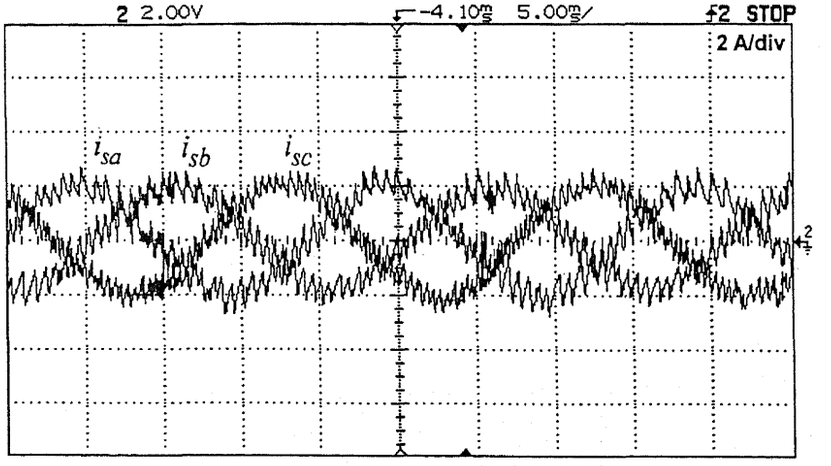


Fig. 3.25 Compensated source currents

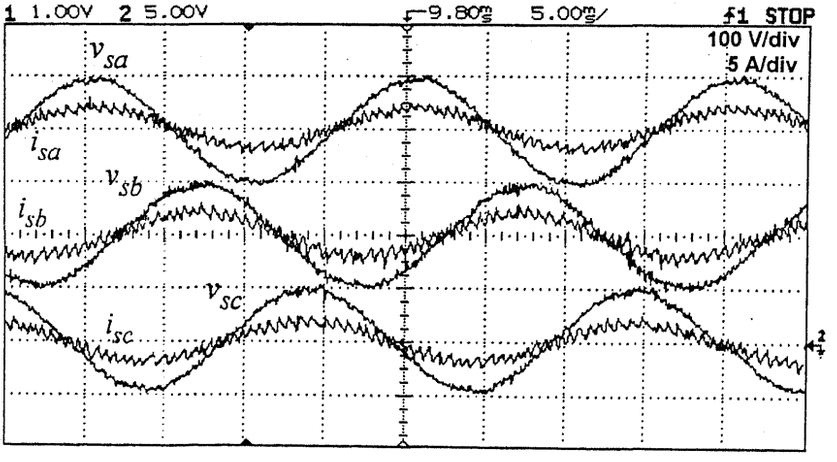


Fig. 3.26 Source currents and voltages

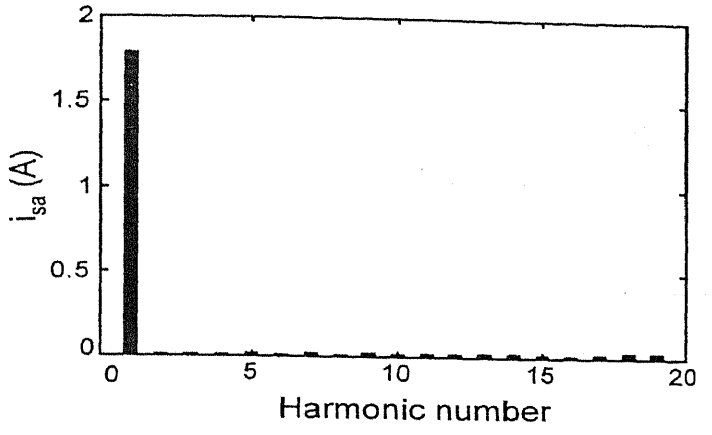


Fig. 3.27 Harmonic spectrum of source current in phase *a*

The dc capacitor voltages are shown in Fig. 3.28. It is seen that the PI voltage control loop regulates the total capacitor voltage to approximately 260 V, which is $2V_{cref}$. Sometimes due to various practical factors (which will be discussed in detail in Chapter 4), the dc capacitors may exhibit minor voltage imbalance problem. However, the problem is solved using band shifting method as discussed in [55].

The reference and actual compensator currents are shown in Fig. 3.29, 3.30 and 3.31 respectively. Their waveforms resemble to those of simulated results as shown in Fig. 3.18 (a), (b) and (c) respectively.

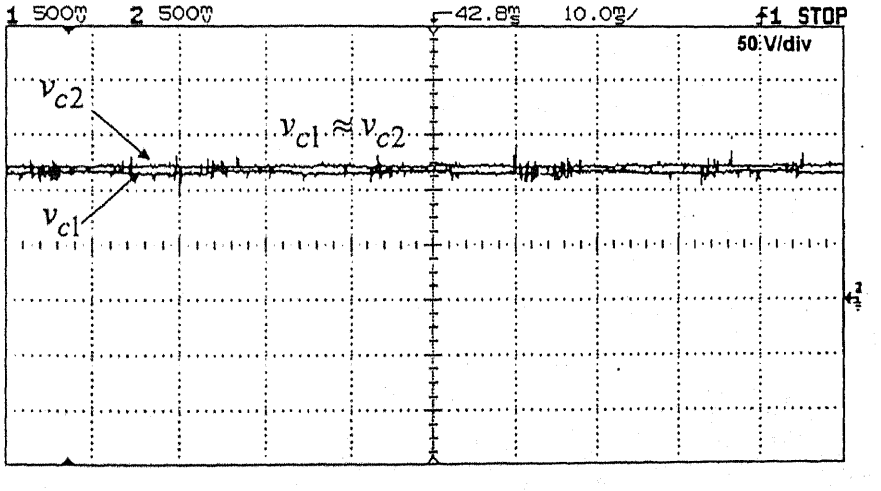


Fig. 3.28 Voltages of dc capacitors

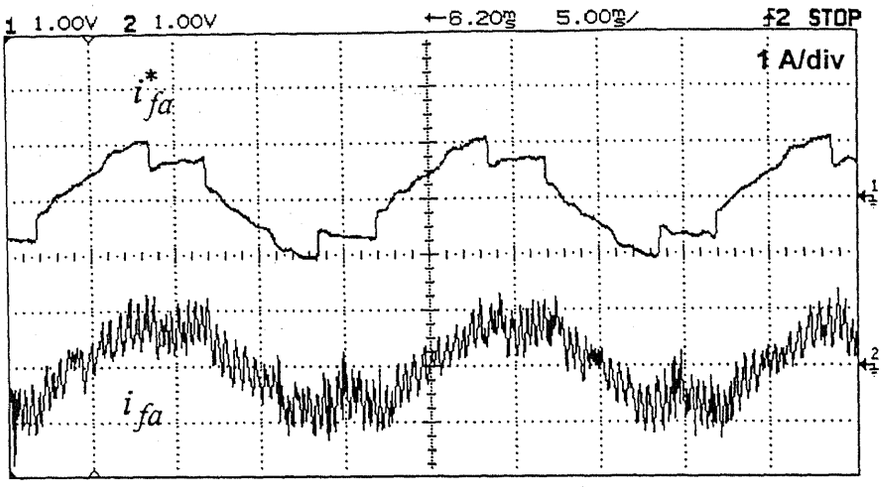


Fig. 3.29 Reference (i^*_{fa}) and actual (i_{fa}) compensator current in phase-*a*

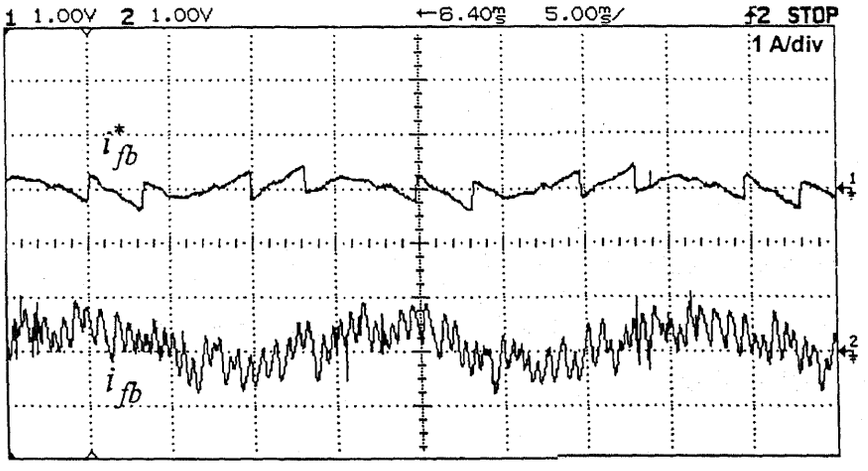


Fig. 3.30 Reference (i^*_{fb}) and actual (i_{fb}) compensator current in phase-*b*

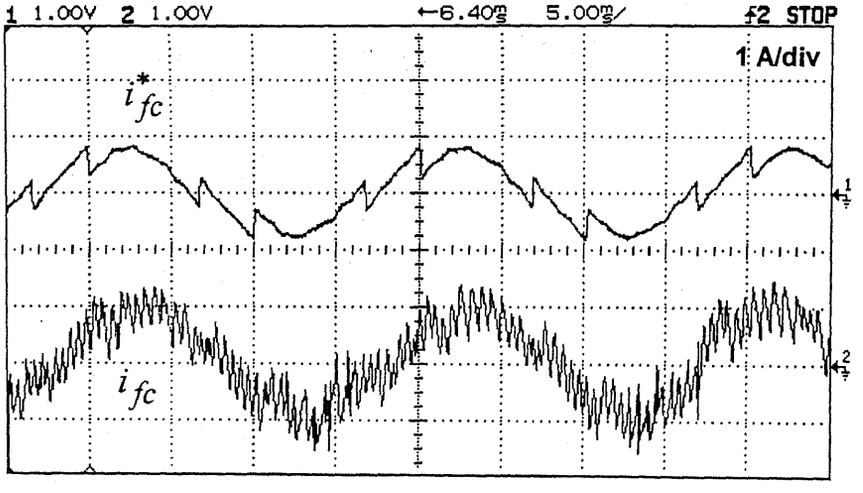


Fig. 3.31 Reference (i^*_{fc}) and actual (i_{fc}) compensator current in phase-*c*

3.10.2 Transient Performance

The transient performance of the compensator is also verified experimentally. In Fig. 3.32, the effect of turning the compensator on/off on source current is recorded. Source current in phase-*a* only has been shown. When the compensator is switched off, source currents are identical to load currents. As soon as compensator is switched on, within one cycle source current settles to steady state value. When compensator is off, the compensator currents are zero (only a compensator current in phase-*a* is shown in Fig. 3.32).

The load transient is created by removing the R-L loads in phases *a* and *b* while keeping the rectifier load. In Fig. 3.33, the source current and load current in phase-*a* are shown. It is observed that when load is R-L plus rectifier, the source current settles to higher value within a cycle. When the load is switched to rectifier load only in phases *a* and *b*, the source current again settles to lower value. The three-phase source currents remain balanced and sinusoidal even under the transient load conditions. The total dc capacitors voltage along with load current in phase-*a* are shown in Fig. 3.34. The rise and dip in v_c can be explained in a way similar to Sub-section 3.9.2. The variation of P_{loss} and load current in phase-*a* are shown in Fig.3.35. Its variation is found to be similar to that shown in Fig. 3.21 (c).

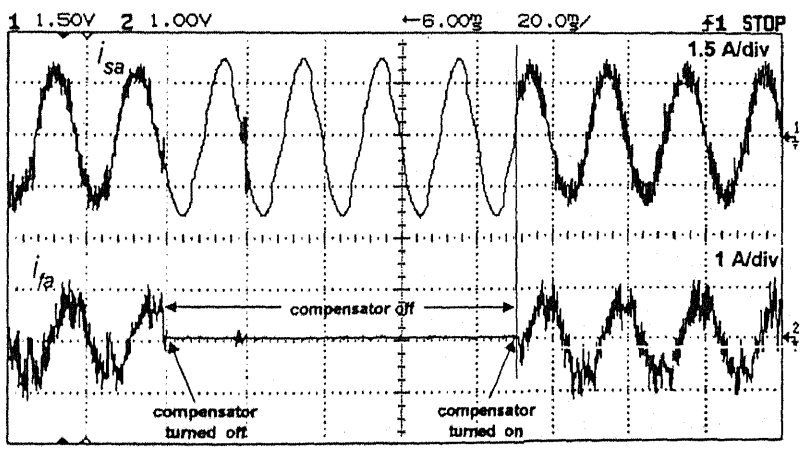


Fig. 3.32 Source current when compensator is switched on or switched off

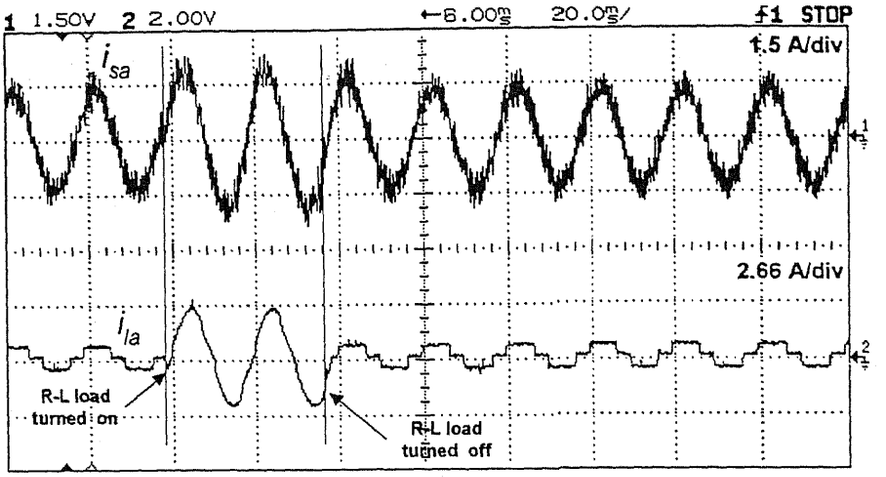


Fig. 3.33 Source current under transient load

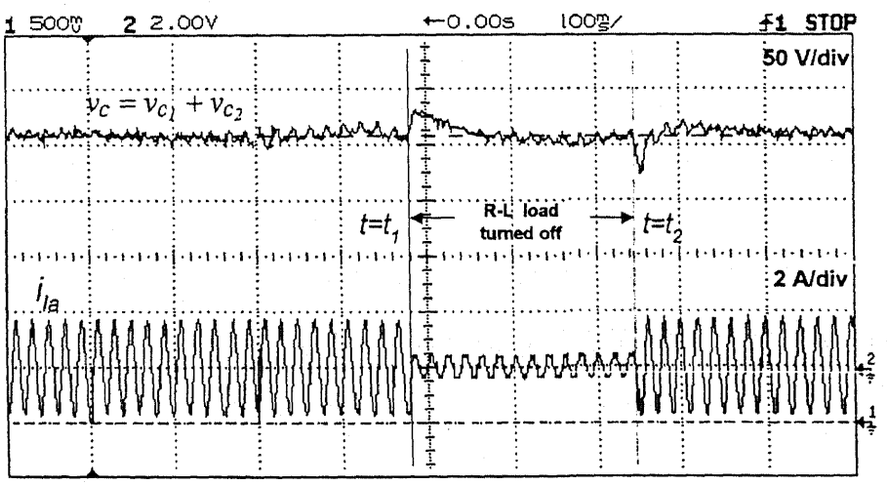


Fig. 3.34 Total dc capacitors voltage under transient load

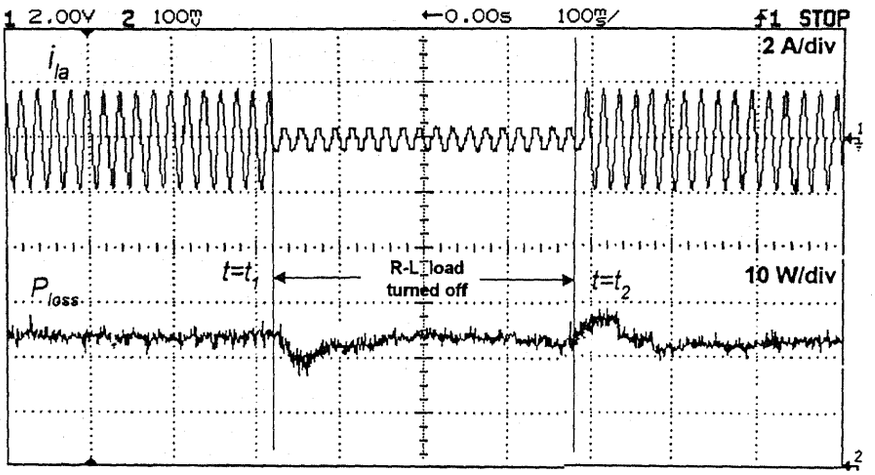


Fig. 3.35 Variation of P_{loss} under transient load

3.11 SIMULATION AND EXPERIMENTAL STUDIES UNDER UNBALANCED SOURCE VOLTAGES

The concept of shunt compensation under unbalanced source voltages has been discussed in Sub-section 2.8.2 of Chapter 2. The simulation and experimental results with ideal inverter have also been presented. It has been demonstrated that the modified algorithm (2.81) gives balanced and sinusoidal source currents even though the source voltages are unbalanced. In this section we verify this algorithm with practical inverter of neutral clamped topology. Both simulation and experimental results are presented below.

3.11.1 Simulation and Experimental Results

The parameters of system are same as given in Section 3.9 and 3.10. The unbalance in source voltages is as following.

$$v_{sa} = 80\sin 100\pi t \text{ V}$$
$$v_{sb} = 100\sin(100\pi t - 2\pi/3 - \pi/6) \text{ V}$$
$$v_{sc} = 65\sin(100\pi t + 2\pi/3) \text{ V}$$

The simulated source current is shown in Fig. 3.36. It is seen that currents are balanced and sinusoidal. Source voltage in phase-*a* (reduced by a scale of 25) has also been plotted in the figure. Source current and voltage in phase-*a* are in phase. Source current and voltage in phase *c* will also be in phase. However, phase-*b* source current and voltage will not be in phase as phase-*b* source voltage has phase unbalance too in addition to magnitude unbalance.

The experimental source current obtained with modified algorithm (2.82), are shown in Fig. 3.37. The current waveforms are similar to that shown in Fig. 3.36. The source voltage and current in phase-*a* are shown in Fig. 3.38.

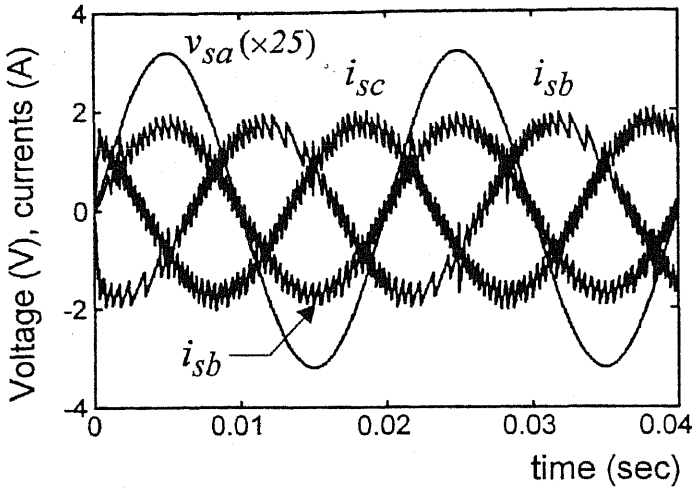


Fig. 3.36 Source currents for unbalanced voltages with modified algorithm

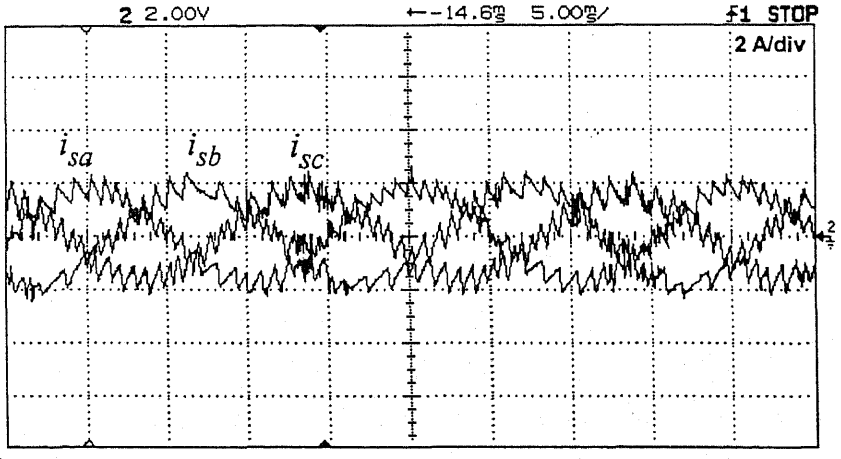


Fig. 3.37 Source currents for unbalanced source voltages with modified algorithm: Experimental

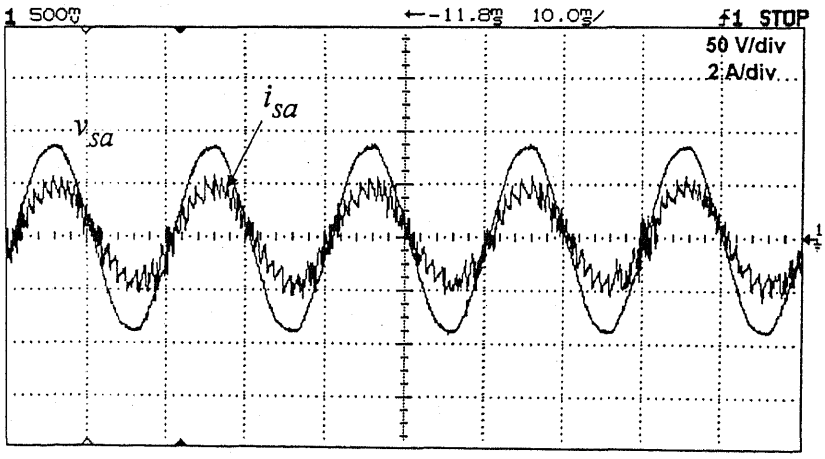


Fig. 3.38 Source current and voltage in phase for unbalanced source voltages with modified algorithm: Experimental

3.12 CONCLUSIONS

In this chapter the various topologies of the DSTATCOM have been presented. A single-phase compensator topology can be employed in two wire supply systems. Single-phase RDCLI topology minimizes the switching losses in the inverter devices, allows higher switching frequencies at reasonably high power level and reduces noise and electromagnetic interference. However it has disadvantages of higher device voltage stresses (when the output voltage is greater than twice the dc input voltage), zero crossing failure unless the initial current in the resonant inductor is built properly. Its three-phase version could be used but it gives utilization difficulties. The single and three phase versions of current source inverter topology are not preferred over voltage source inverter topology due to less efficiency and higher initial cost. The three-leg, three capacitors DSTATCOM topology is not suitable, as its compensated source currents are not balanced. If a single dc storage capacitor is employed in stead of three, it results in the shorting of the dc capacitor. This is overcome by a topology with three independent single-phase inverters with isolation transformers, which prevents the shorting of the capacitor. But this topology is not suitable for loads containing dc. A three-phase, three-leg DSTATCOM topology is suitable for ac load compensation but not suitable for loads containing dc components as it causes voltage imbalance of dc capacitors. A three-phase, four-leg inverter topology (Fig. 3.11) does not pose this problem as it has single dc storage capacitor. It can compensate ac as well as dc load. However it needs high bandwidth and therefore increases the switching losses. Also it adds high switching frequency components into the system through the neutral path.

A neutral clamped inverter topology is suitable for independent tracking of three-phase reference currents. But if the zero sequence currents in neutral path contains dc component the voltage of the two capacitors become unbalanced. This topology is chosen for ac load compensation for balanced and unbalanced source voltages with algorithms proposed in Chapter 2. The detailed simulation and experimental results have been presented with inverter circuit. A closed loop control of total dc capacitor voltage is described. The algorithm presented in this chapter has been validated through simulation and experiments running C/C++ programs in real time.

CHAPTER 4

DSTATCOM TOPOLOGY FOR LOADS CONTAINING DC AND AC

In the previous chapter, various DSTATCOM topologies of shunt compensators have been described. The merits and demerits of each topology were discussed in detail. The neutral clamped topology [38] was chosen for ac load compensation for balanced as well as unbalanced voltages and has been described in Chapter 3. However this topology is not suitable for loads containing dc components as the dc capacitors will exhibit the voltage imbalance in dc capacitors. In this chapter, the problem of voltage imbalance in dc capacitors has been studied in detail. To overcome the voltage imbalance problems, a new DSTATCOM topology [58] has been proposed. This topology may be referred to as the Neutral Clamped Inverter-Chopper compensator topology. It is suitable for load balancing and power factor correction in loads containing ac and dc components. Its state space model is derived and various chopper control schemes are discussed to regulate the each dc capacitor voltage close to the reference value. The detailed simulation results are presented to verify the effectiveness of the compensator for unbalance loads containing ac and dc components and harmonics. The experimental results are also given.

4.1 DSTATCOM TOPOLOGY FOR DC LOADS

The compensator uses a current source comprising of a voltage source inverter (VSI) with six switches ($S_1 - S_6$), operated in a hysteresis band current control scheme (Fig. 4.1). The compensator is directly coupled to the ac system through the interface inductor L_f that also has a resistance R_f. The topology contains two dc storage capacitors as shown in Fig. 4.1. In this circuit, the junction (n') of the two capacitors is connected to the neutral of the load. This configuration of compensator allows a path for the zero-sequence current and therefore the three injected currents can be independently controlled. Note that the inverter configuration is identical to that described in Section 3.6. This inverter topology is extended

by the addition of chopper circuit that is represented by the switches S_7 and S_8 with anti-parallel diodes and the chopper inductance L_{ch}-R_{ch} as shown in Fig. 4.1. The purpose of this circuit is to balance the voltages of the two capacitors, C_1 and C_2 by injecting a current i_{ch} at the node n'. The voltage imbalance in capacitors may arise due to factors discussed later in this chapter.

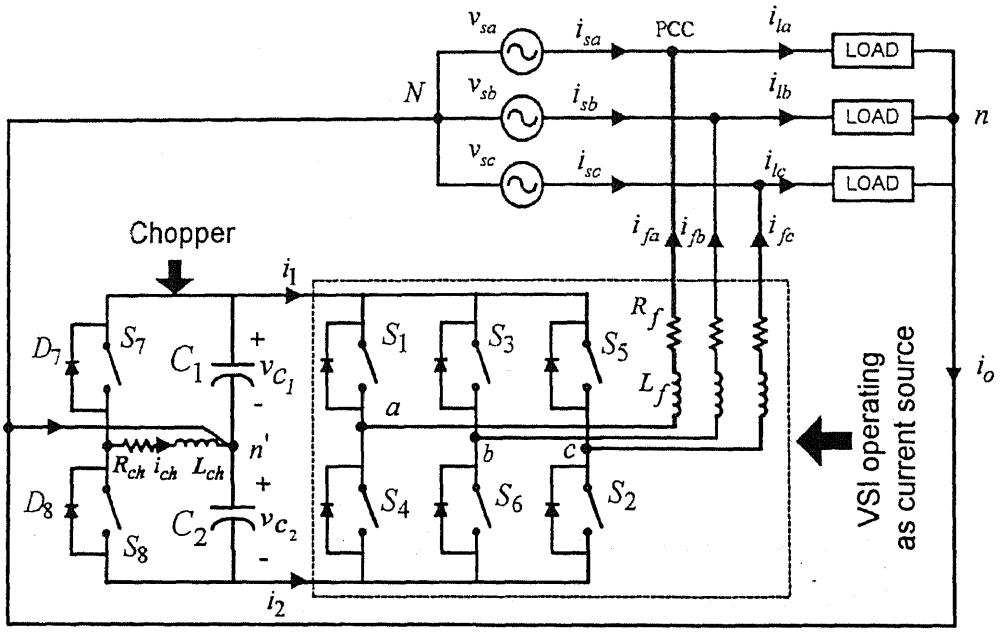


Fig. 4.1 A compensator structure in which a neutral-clamped three-phase VSI is used

The topology given in Fig. 4.1 can be compared with the three-phase, four-leg topology described in Section 3.5 (Fig. 3.11). This topology also uses 8 switches but the capacitor is not split into two. It is therefore equivalent to disconnecting the junction of the two capacitors in Fig. 4.1 from node n' and treating the series combination of C_1 and C_2 as a single capacitor. An advantage of using the spilt capacitors connected as shown in Fig. 4.1 is that the high frequency components of the neutral current i_o are not passed to the system neutral via path $n-N$. Instead these components are automatically routed via path $n-n'$, C_1 and C_2 into the inverter currents i_1 and i_2 respectively. This filtering action is due to C_1, C_2 and L_{ch} and it is independent of the reference current for i_{ch}. The reference for i_{ch} may be set to negative of the average load neutral current, $-I_o$, without passing high frequency component of neutral current to the system neutral. This reduces the bandwidth

requirement on the chopper consisting of the switches of the fourth leg ($S_7 - S_8$), and consequently the switching losses.

In the chopper circuit of Fig. 4.1, the anti-parallel diodes D_7 and D_8 are shown across each chopper switch. Let us define the voltages across C_1 and C_2 by v_{c1} and v_{c2} respectively. Normally the switches S_7 and S_8 are kept open. Now suppose the voltage v_{c1} drops and v_{c2} rises. The switch S_8 is then closed such that a current is built up in the inductor L_{ch}. This mode of operation of chopper is shown in Fig. 4.2. Once the current reaches a certain level, the switch S_8 is opened. The inductor current then discharges through the diode D_7 to bring up the voltage v_{c1} to the desired level. The chopper in this mode is shown in Fig. 4.3. Similarly, the charge can be transferred from the capacitor C_1 to the capacitor C_2 by closing the switch S_7 to build current in L_{ch} and then charging C_2 through the diode D_8 by opening the switch S_7. The feedback control of this chopper circuit is essential for the success of the scheme. The various schemes of chopper control to equalize the voltage of the capacitors will be described in this chapter. The reference current generation scheme and closed loop dc capacitor voltage control of the compensator are same as discussed in Section 3.7 (Fig. 3.13) and are assumed to be in operation concurrently with chopper. The detailed simulation results have been presented. The experimental results have been given to verify simulation results.

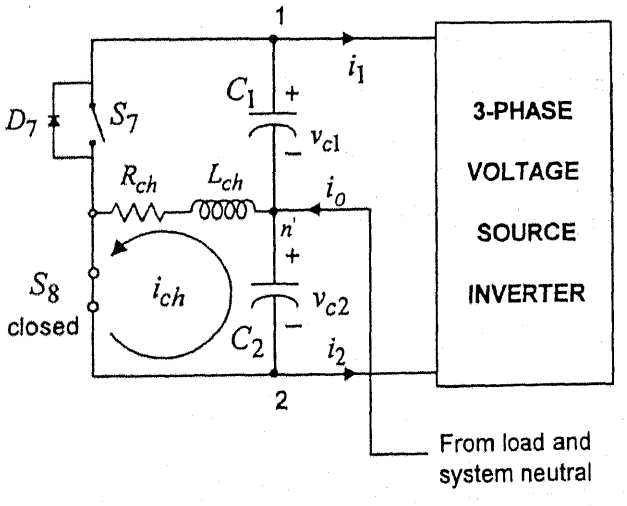


Fig. 4.2 Equivalent circuit when chopper switch S_8 is closed

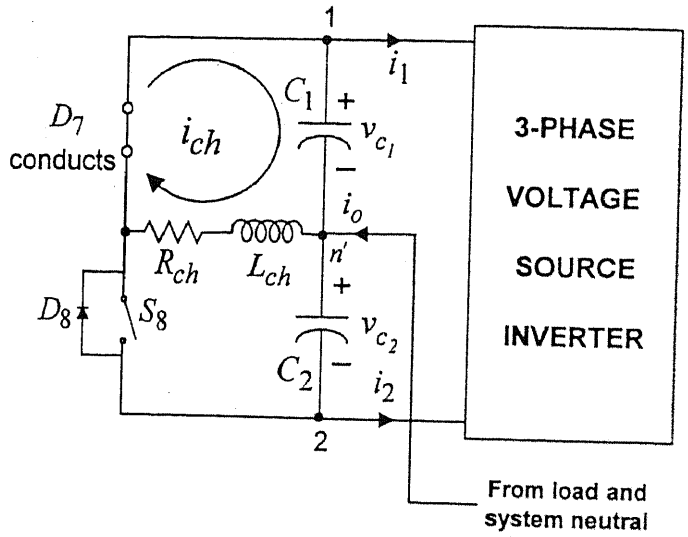


Fig. 4.3 Equivalent circuit when chopper switch S_8 is opened and D_7 conducts

4.2 STATE SPACE MODEL FOR COMPENSATOR INCLUDING CHOPPER

The state space model for neutral clamped inverter topology has been discussed in Sectio 3.8. All the conventions and variables assumed there also apply in this section. However, i the inverter-chopper topology there is one more state variable, the chopper current (i_{ch}) an two logical variables S_u and S_l for the control of switches S_7 and S_8 respectively Therefore the order of the system matrix becomes 6. The equations (3.6)-(3.12) developec in Section 3.8 are valid here. Equations (3.13)-(3.14) are not valid because of choppe current and are replaced by new equations derived below. In addtion to this, one more state equation for time derivative of chopper current is included in the model.

The complete equivalent circuit of chopper is shown in Fig 4.4, where, i_1 and i_2 are given by (3.6)-(3.7).

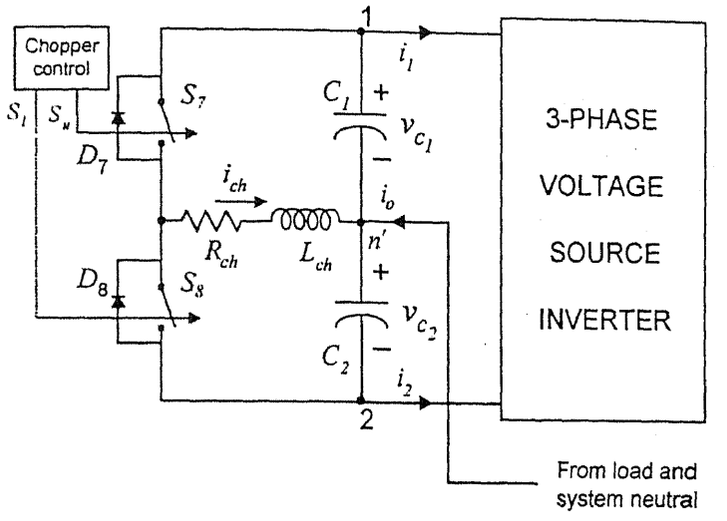


Fig. 4.4 Equivalent circuit of chopper

In Fig. 4.4, the switch S_7 can be closed and S_8 opened or vice versa. In each case KCL can be applied at nodes 1 and 2, and KVL can be applied around the loop of the closed switch. The resulting equations can be combined with the help of (3.6) and (3.7) and binary variables S_u and S_l to obtain the following assuming $C_1 = C_2 = C$.

$$\frac{dv_{c1}}{dt} = -S_a \frac{i_{fa}}{C} - S_b \frac{i_{fb}}{C} - S_c \frac{i_{fc}}{C} - P_{13} \frac{i_{ch}}{C} \tag{4.1}$$

$$\frac{dv_{c2}}{dt} = \overline{S}_a \frac{i_{fa}}{C} + \overline{S}_b \frac{i_{fb}}{C} + \overline{S}_c \frac{i_{fc}}{C} + P_{23} \frac{i_{ch}}{C} \tag{4.2}$$

$$\frac{d_{i_{ch}}}{dt} = -\frac{R_{ch}}{L_{ch}} i_{ch} + P_{13} \frac{v_{c1}}{L_{ch}} - P_{23} \frac{v_{c2}}{L_{ch}} \tag{4.3}$$

where P_{13} and P_{23} are binary variables given by,

$$P_{13} = \overline{S}_l \bullet \left\{ S_u + (\overline{sign} \bullet mag) \right\} \tag{4.4}$$

$$P_{23} = \overline{S}_u \bullet \left\{ S_l + (sign \bullet mag) \right\} \tag{4.5}$$

Here the symbol $\bullet$ and $+$ are logical AND and OR operators respectively. In logical expressions the terms in (4.4) and (4.5) are explained as

$$sign=\begin{cases}1 & for\ i_{ch}>0\\ 0 & for\ i_{ch}\le 0\end{cases},\qquad mag=\begin{cases}1 & for\ |i_{ch}|>0\\ 0 & for\ |i_{ch}|=0\end{cases} \tag{4.6}$$

When S_7 and S_8 are both off, i_{ch} may exist transiently. If $i_{ch}>0\,(<0)$, it will flow through diode across S_8 (S_7). If i_{ch} reaches zero value and it will not build up again until chopper is re-activated. The variables *sign* and *mag* in (4.4)-(4.5) ensure correct values of P_{13} and P_{23} in this case.

Through (3.10)-(3.12) and (4.1)-(4.3), we obtain the following state space model

$$\frac{d}{dt}\begin{bmatrix}x_1\\ x_2\end{bmatrix}=\begin{bmatrix}A_{11} & A_{12}\\ A_{21} & A_{22}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}B_1\\ B_2\end{bmatrix}u \tag{4.7}$$

where,

$$x_1=[i_{fa}\quad i_{fb}\quad i_{fc}]^t,\ x_2=[v_{c_1}\quad v_{c_2}\quad i_{ch}]^t,\ u=[v_{sa}\quad v_{sb}\quad v_{sc}]^t$$

and

$$A_{11}=\begin{bmatrix}-R_f/L_f & 0 & 0\\ 0 & -R_f/L_f & 0\\ 0 & 0 & -R_f/L_f\end{bmatrix}\qquad A_{12}=\begin{bmatrix}S_a/L_f & -\bar{S}_a/L_f & 0\\ S_b/L_f & -\bar{S}_b/L_f & 0\\ S_c/L_f & -\bar{S}_c/L_f & 0\end{bmatrix}$$

$$A_{21}=\begin{bmatrix}-S_a/C & -S_b/C & -S_c/C\\ \bar{S}_a/C & \bar{S}_b/C & \bar{S}_c/C\\ 0 & 0 & 0\end{bmatrix}\qquad A_{22}=\begin{bmatrix}0 & 0 & -P_{13}/C\\ 0 & 0 & P_{23}/C\\ P_{13}/L_{ch} & -P_{23}/L_{ch} & -R_{ch}/L_{ch}\end{bmatrix}$$

$$B_1=\begin{bmatrix}-1/L_f & 0 & 0\\ 0 & -1/L_f & 0\\ 0 & 0 & -1/L_f\end{bmatrix}\qquad B_2=\begin{bmatrix}0\end{bmatrix}_{3\times 3}$$

4.3 VOLTAGE IMBALANCE IN CAPACITORS

The compensator topology of Fig. 4.1 employs two capacitors for generating two levels of voltages. More capacitors are used in multi level inverters with higher number of voltage levels. Unfortunately however, the capacitors in such compensator topologies are associated with the problem of voltage imbalance [54, 56-57, 59]. This problem may be classified into two categories, minor and major voltage imbalance. The minor voltage imbalance problem arises due to practical factors when load does not have dc component. The following practical factors are responsible for small imbalance in the capacitor voltages [53, 56].

- Unequal capacitance leakage currents
- Unequal delays in the semiconductor devices
- Asymmetrical charging of the capacitors during transients
- Asymmetrical circuit configuration (due to measurement and signal conditioning circuit)

The minor voltage imbalance problem has been discussed in [54, 56-57]. These references also provide guidelines to the remedial actions that can be taken to alleviate this problem, such as changing the switching instants (of gating signals S_1 to S_6 in Fig. 4.1) in a direct or indirect manner so as to achieve the voltage balance.

However, when the load current contains any dc component, the capacitors are associated with major voltage imbalance [58]. For this case, the methods suggested above will fail to deliver due to the limit imposed on the switching instants. Beyond that limit, the tracking of reference current will be affected. To correct for any major voltage imbalance, the chopper is included in the compensator circuit of Fig. 4.1.

When the compensator is working perfectly, the current i_o (Fig. 4.1) flows through path $n-n'$, and the sum of i_{sa}, i_{sb}, i_{sc} is zero. Considering all kinds of unbalances in load, and steady state operation, current i_o can be assumed to be a non-sinusoidal periodic waveform. In general, the spectrum of i_o may contain a dc component, supply frequency component, and its harmonics, i.e.,

$$i_o = i_{la} + i_{lb} + i_{lc} = I_o + \sum_{h=1,2,3...}^{\infty} I_h \sin h(\omega t + \phi_h) \tag{4.8}$$

The second term on the right hand side of (4.8) is responsible for generating ripples in capacitor voltages at fundamental and harmonic frequencies. For large values of capacitors, these ripples are small and do not cause any problems. However the effect of the first term, I_o, which is the dc part of i_o, is significant, as it is directly responsible for causing the voltage imbalance. A feedback loop regulates the sum of the capacitor voltages, $v_{c1} + v_{c2}$, to be a constant which is equal to $2V_{cref}$. From equivalent circuit of Fig. 4.4, if $S_u = S_l = 0$ and $i_{ch} = 0$, we have

$$\frac{dv_{c1}}{dt} = -\frac{i_1}{C} \tag{4.9}$$

$$\frac{dv_{c2}}{dt} = \frac{i_2}{C} \tag{4.10}$$

Combining (4.9) and (4.10) we get

$$\frac{d(v_{c1} + v_{c2})}{dt} = -\frac{i_1 - i_2}{C} \tag{4.11}$$

The total capacitor voltage $v_c = v_{c1} + v_{c2}$ is regulated to a constant value by the PI controller. Therefore from (4.11) we get $i_1 = i_2$ and hence applying KCL at node n' of Fig. 4.4 we obtain $i_1 = i_2 = i_o/2$. Again from (4.9) and (4.10), we can conclude that v_{c1} and v_{c2} will contain ripple voltages at supply frequency, its harmonics and possibly other harmonics generated by the load. However, if C_1 and C_2 are large capacitors, these ripples are negligible. But the positive or negative dc components in i_o will monotonically decrease the value of v_{c1} and increase the value of v_{c2} or vice versa respectively over several cycles.

Using (4.9) and (4.10),

$$v_{c1} \approx V_{c1} = V_{c10} - \frac{I_o}{2C}t \tag{4.12}$$

$$v_{c2} \approx V_{c2} = V_{c20} + \frac{I_o}{2C}t \tag{4.13}$$

where, t is time in seconds, V_{c1} and V_{c2} are average values of v_{c1} and v_{c2} respectively. At $t = 0$, $v_{c1} = V_{c10}$ and $v_{c2} = V_{c20}$. In general, $V_{c10}, V_{c20} \neq V_{cref}$. Thus, the capacitors may have unequal initial voltages and voltage drift due to I_o. It is also clear that if I_o is sufficiently large, in few cycles V_{c1} or V_{c2} goes below the peak of the system ac voltage and the tracking of reference compensator currents will be affected. If I_o is small, it will lead to voltage imbalance in dc capacitors after several cycles. Hence it is necessary to regulate the voltage of each capacitor to a reference value (V_{cref}), when three phase load draws current such that $I_o \neq 0$. In the present work, a two-quadrant chopper has been employed to regulate the voltage of each capacitor. The six different control schemes [58-60] are discussed. In principle, the chopper is required in steady state to generate a current, i_{ch}, whose average value (I_{ch}) is equal and opposite to the average value of i_o. Effectively it means that the current I_o is bypassed around the capacitors C_1, C_2 through switch-diode combination $S_7 - D_7$ and $S_8 - D_8$.

4.4 SYSTEM CONFIGURATION

In this section, the system of Fig. 4.1 has been simulated using MATLAB using the state space model (4.7). The system parameters are tabulated in Table 4.1. The load currents for the system are shown in Fig. 4.5. It can be clearly seen that all of them have an offset (dc). The neutral current (i_o) is also shown in the figure. It has an average value (I_o) of 3.3 A.

The block diagram of the control system is given in Fig. 3.13. From the given source voltages and load currents, the reference currents i_{fa}^*, i_{fb}^* and i_{fc}^* are generated using (3.2). In this algorithm, β is set to 0 for unity power factor operation. The load average power $\bar{p}_l$ in (3.2) is computed using moving average filter [46] over half cycle. The P_{loss} term is computed using PI controller (Fig. 3.13), with K_p and K_i as given in the Table 4.1. The P_{loss} term is updated once in a cycle. The state space model of the inverter-

chopper given in Section 4.2 has been used to compute the actual filter currents, capacitor voltages and chopper current. Once we know the actual and the reference filter currents, the VSI is operated in order to track them in the hysteresis band. In the following sections, the effect of dc load on the performance of the compensator is described. It is shown that dc component of load results in poor performance of the compensator. To retain the correct performance of the compensator, six different schemes of chopper control are then described in Sections 4.6 and 4.7.

Table 4.1 System parameters

System Parameters	**Values**
Source voltages	360 V (peak), balanced and sinusoidal
Load	◆ $R_a = 26\Omega$, $R_b = 35\Omega$, $R_c = 100\Omega$ ◆Three-phase half bridge diode rectifier with highly inductive load drawing an output current of 3.3 A
DC capacitors	$C_1 = C_2 = 2200$ μF
Interface inductor	$R_f = 2\Omega$, $L_f = 20$ mH
PI controller gains	$K_p = 10$, $K_i = 1$
Chopper inductors	$L_{ch} = 20$ mH, $R_{ch} = 2\Omega$
Reference voltage	$V_{cref} = 500$ V
Hysteresis band	Compensator: ± 1 A, Chopper: ± 0.2 A

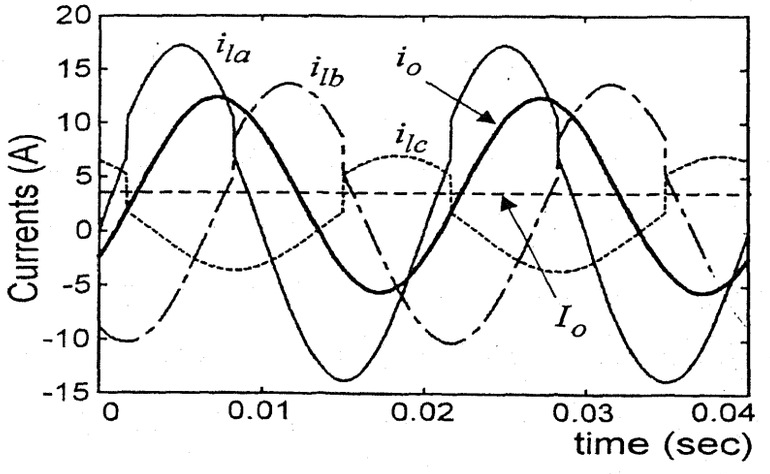


Fig. 4.5 Load currents with dc component

4.5 OPERATION WITHOUT CHOPPER

In this simulation, the switches S_7 and S_8 are assumed to be off. The effect of the dc component in the neutral current shown in Fig. 4.5 is to discharge and charge the capacitors C_1 and C_2 respectively as per (4.12)-(4.13). The effect on the voltage of the capacitors and tracking performance is shown in Fig. 4.6 and 4.7 respectively.

Due to presence of the positive I_o, v_{c1} decreases and v_{c2} increases continuously as per equations (4.12)-(4.13) from initial value of 500 V. However, (4.12) and (4.13) remain operative only till the current tracking is faithful. When tracking is lost, the neutral current i_o (Fig. 4.1) bypasses the compensator and enters the system neutral (N) making (4.12)-(4.13) inoperative. It is observed that beyond 10 cycles i.e. $t = 0.2$ sec, v_{c1} and v_{c2} (Fig. 4.6) do not decrease and increase at the same rate. After $t = 0.2$ sec, v_{c2} becomes constant and tracking does not remain faithful. As a consequence of loss of tracking, voltages v_{c1} and v_{c2} stabilize to 300 and 700 V respectively after 100th cycle (Fig. 4.6), instead of the reference value of 500 V. The two dc storage capacitors which act as energy reservoir to VSI, are directly connected to point of common coupling (PCC) through interface inductor. Due to this arrangement, the capacitor voltages do not increase or decrease monotonically. One of the capacitor voltages settles around the peak of the ac system voltage (v_{peak}). The other one has voltage ($2V_{c\,ref} - v_{peak}$).

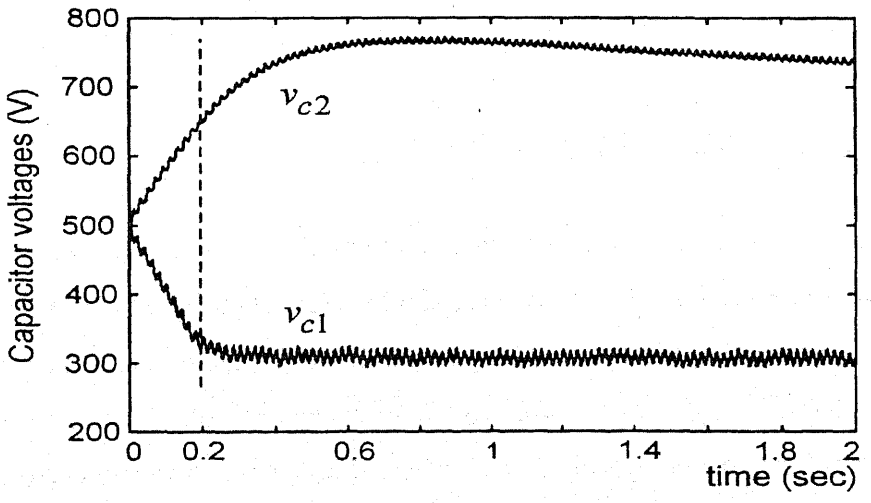


Fig. 4.6 Voltage imbalance in dc capacitors

Fig. 4.7 shows the steady state tracking performance over one cycle of supply voltage where the capacitor voltages reach steady state. To compare the nature of voltage and current waveforms in the same graph, the voltages in Fig. 4.7 are scaled down by 50. From Fig. 4.7, it is observed that between points p and q tracking is lost as voltage, v_{c1} is close to source voltage v_{sa}. As a consequence of this the compensator is unable to track sudden change in reference current (i^*_{fa}) between points p and q. It is observed that between points r and s, v_{c1} is less than v_{sa} therefore the current i_{fa} has negative slope. Later, after point q, v_{sa} is smaller than v_{c1} and therefore tracking is regained for rest of the voltage cycle. In summary, the operation without chopper results in highly unequal capacitor voltages (300 V, 700 V) and distorted filter currents resulting in imperfect compensation.

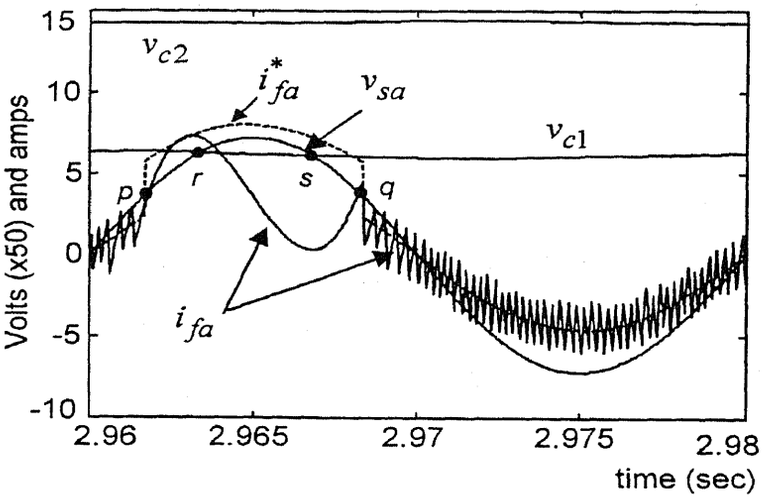


Fig. 4.7 Effect of dc component of load on tracking performance

4.6 CONTROL SCHEMES OF CHOPPER

The various control schemes of the two-quadrant chopper to regulate the capacitor voltages under dc load are described below. These are single pulse control [58] based on state space model, single pulse control based on energy balance, multi-cycle control, open loop duty cycle control [59], PI duty cycle control and hysteresis control [60]. There are two kinds of control schemes for chopper (i) Voltage control schemes (ii) Voltage and current controlled

schemes. The single and multi-cycle controls come under voltage control schemes, while as PI duty cycle control and hysteresis control come under voltage and current controlled schemes of chopper. For each control schemes the simulation results are presented. For hysteresis control schemes, experimental results are also given.

4.6.1 Single Pulse Control of Chopper

The switches S_7 and S_8 are normally open in Fig. 4.4. Let us assume that the current i_o has a positive dc component, as a result of which v_{c1} drops and v_{c2} rises. A control circuit senses the capacitor voltage v_{c2} and compares it with V_{cref} in a hysteresis band. If the voltage v_{c1} is found to be outside this band, the chopper is activated. The total voltage across C_1 and C_2 is kept constant by the PI controller through the P_{loss} term in (3.2). The chopper executes a single pulse on/off control. The time intervals t_{8on} and t_{8off} in Fig. 4.8 are calculated using the state space model, such that voltage of C_1 changes from the initial value v_{c1}^{cyl} to the final value v_{cref} at the end of the interval $(t_{8on}+t_{8off})$. The state trajectories for capacitor voltages and chopper current are shown in Fig. 4.9.

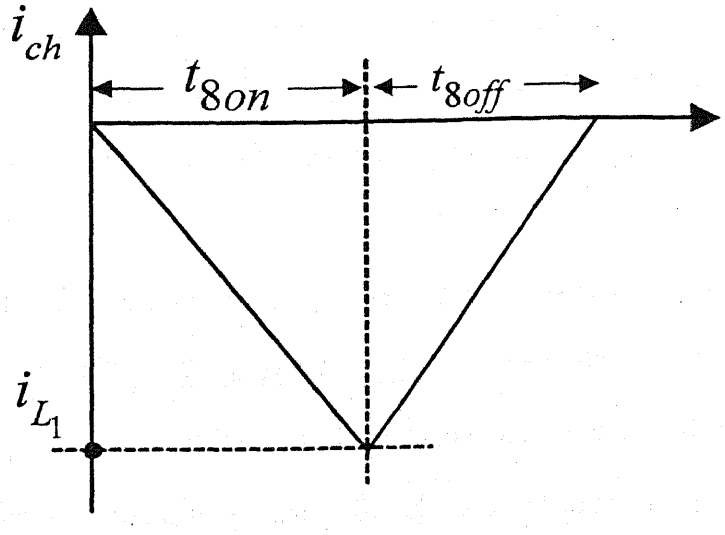


Fig. 4.8 Variation of chopper current

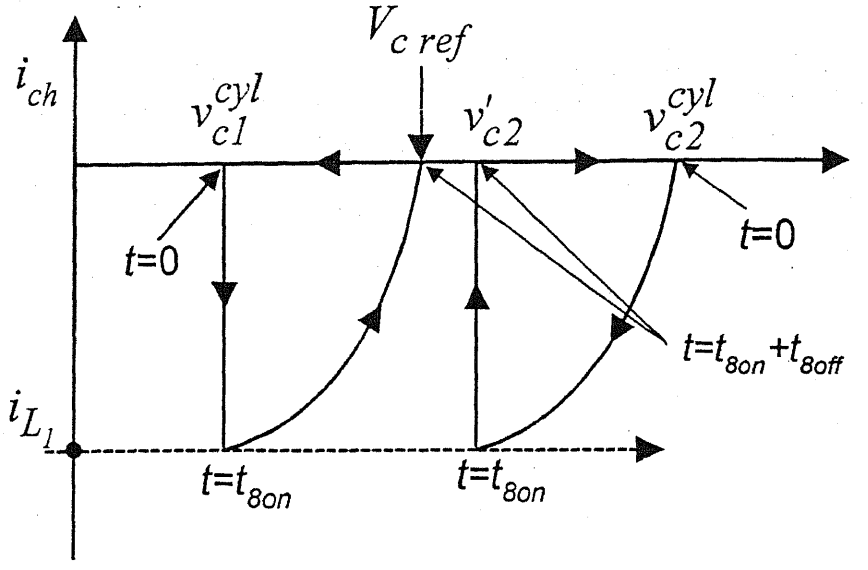


Fig. 4.9 State trajectories of capacitor voltages and chopper current

The chopper action for a positive dc component in i_o consists of closing S_8 (Fig. 4.2) such that a current is built up in the inductor L_{ch} in Fig. 4.4. The switch S_8 is opened after pre-calculated time t_{8on}. The inductor current then discharges through D_7 (Fig. 4.3) to bring up the voltage v_{c1} to the desired level, $V_{c\,ref}$. Switch S_7 is kept off throughout this mode of chopper operation. Similarly for a negative dc component, the charge can be transferred from capacitor C_1 to capacitor C_2 by closing the switch S_7 to build current in L_{ch} and then charging C_2 through D_8 by opening S_7 while keeping S_8 off throughout this period.

In Fig. 4.4, i_1 and i_2 are the circulating currents in the inverter-capacitor loop. In order to determine an analytical expressions for $t_{8\,on}$ and $t_{8\,off}$, the system equations in (4.7) are approximated as follows. It is assumed that during the time $(t_{8\,on}+t_{8\,off})$, the rate of monotonic change in capacitor voltages due to i_1 and i_2 is small. The chopper is assumed to restore the voltages to values close to $V_{c\,ref}$ at a fast rate. Therefore i_1 and i_2 in Fig. 4.4 are neglected. Under this assumption, the capacitor voltages and chopper currents are described by $\dot{x}_2 = A_{21}x_1 + A_{22}x_2 \approx A_{22}x_2$. Further the 3×3 matrix A_{22} reduces to a

size of 2×2, as only one switch S_7 or S_8 is closed and the other is open. The system equations, when S_7 is closed and S_8 is open, are given by

$$\frac{d}{dt}\begin{bmatrix} v_{c1} \\ i_{ch} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C} \\ \frac{1}{L_{ch}} & -\frac{R_{ch}}{L_{ch}} \end{bmatrix} \begin{bmatrix} v_{c1} \\ i_{ch} \end{bmatrix} \triangleq A_{S7} \begin{bmatrix} v_{c1} \\ i_{ch} \end{bmatrix} \tag{4.14}$$

with v_{c2} being constant. Similarly when S_8 is closed and S_7 is open the system equations are given by

$$\frac{d}{dt}\begin{bmatrix} v_{c2} \\ i_{ch} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L_{ch}} & -\frac{R_{ch}}{L_{ch}} \end{bmatrix} \begin{bmatrix} v_{c2} \\ i_{ch} \end{bmatrix} \triangleq A_{S8} \begin{bmatrix} v_{c2} \\ i_{ch} \end{bmatrix} \tag{4.15}$$

with v_{c1} remaining constant. The equations (4.14)-(4.15) describe the approximate dynamics of the state vector x_2.

Let i_o have a positive dc component. Therefore S_8 is closed to build the current i_{ch}. The state transition matrix $\varphi(t)$ when S_8 is closed and S_7 is open, is given by

$$\varphi_{S_8\ on}(t) = \exp(A_{S8}\,t) = \begin{bmatrix} a_{11}(t) & a_{12}(t) \\ a_{21}(t) & a_{22}(t) \end{bmatrix} \tag{4.16}$$

and its elements are given as

$$a_{11}(t) = (\omega_n/\omega_d)\, e^{-\xi\omega_n t}\left[-\sin(\omega_d t-\phi)+2\xi\sin(\omega_d t)\right]$$

$$a_{12}(t) = (1/\omega_d\, C)\, e^{-\xi\omega_n t}\sin(\omega_d t)$$

$$a_{21}(t) = -(1/\omega_d\, L_{ch})\, e^{-\xi\omega_n t}\sin(\omega_d t)$$

$$a_{22}(t) = -(\omega_n/\omega_d)\, e^{-\xi\omega_n t}\sin(\omega_d t-\phi)$$

where, $\phi = \tan^{-1}\sqrt{1-\xi^2}/\xi;\quad \xi<1,\ \omega_d = \omega_n\sqrt{1-\xi^2}\ ,\ \omega_n = 1/\sqrt{L_{ch}\,C}$

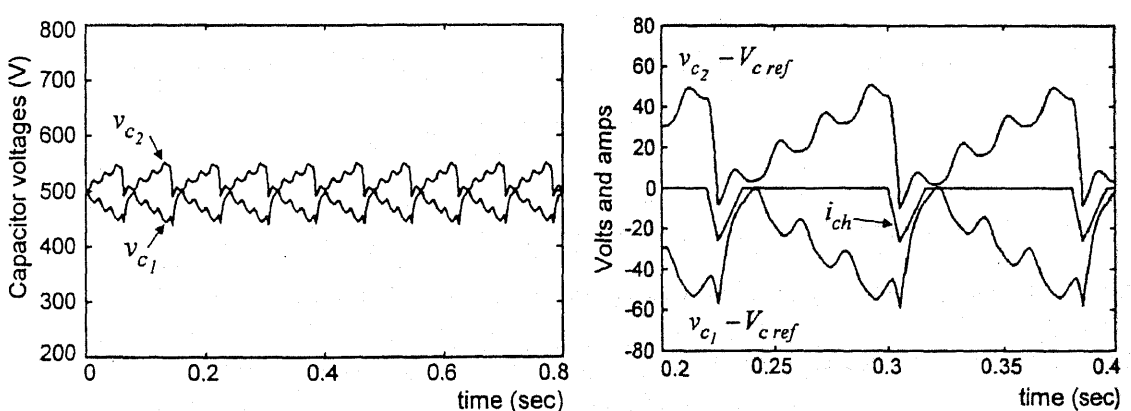
$$I_{L_1} = a_{11}(t_{8\,on})\, v_{c2}^{cyl} \tag{4.22}$$

$$v'_{c2} = a_{21}(t_{8\,on})\, v_{c2}^{cyl} \tag{4.23}$$

With I_{L_1} computed from (4.20) and pre-computed values of a_{11}, and v_{c2}^{cyl}, we compute $t_{8\,on}$. Thus the required on time of the chopper has been computed. It is to be noted that v'_{c2} computed from (4.23) may not be exactly V_{cref}. Its value will depend on the system dynamics. However it is close to V_{cref}.

The above derivation has been carried out assuming i_o has a positive dc component. Similar analysis is valid when i_o has a negative dc component. In that case the roles of v_{c1} and v_{c2} are reversed. Therefore (4.18)-(4.23) can be used with subscripts 1 and 8 replaced by 2 and 7 respectively and reversing the sign of a_{21}. For example v_{c1}^{cyl} and $t_{8\,on}$ are replaced by v_{c2}^{cyl} and $t_{7\,on}$ respectively.

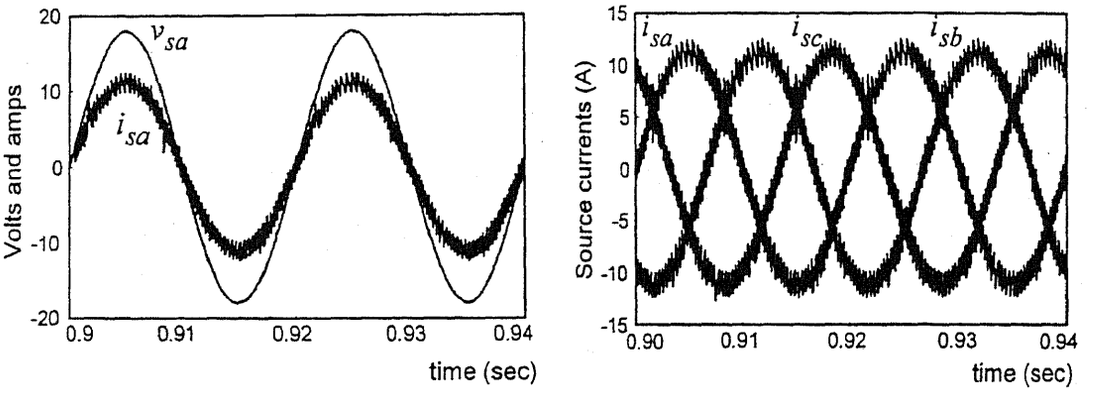
For the system configuration and parameters given in Table 4.1, the operation of the compensator is validated through digital simulation. The dynamics of compensator is modeled by solving the state space model discussed in Sections 4.4. The switching of the inverter is done by monitoring the reference and the actual currents and comparison of error with a hysteresis band. When chopper is activated using single pulse on/off control, the voltages v_{c1} and v_{c2} are regulated close to V_{cref}, albeit with a small ripple. This is shown in Fig. 4.10 (a). Therefore the chopper is able to stabilize the voltages v_{c1} and v_{c2}.



(a) (b)

Fig. 4.10 (a) Capacitors voltage (b) Voltage ripples and chopper current

The voltages v_{c1} and v_{c2} are checked at the positive going zero crossings of voltage v_{sa}. The chopper switch S_7 (S_8) is activated if v_{c1} (v_{c2}) > V_{cref} (zero hysteresis band). Single pulse control brings the capacitor voltage back towards V_{cref}. It is seen in Fig. 4.10 (a) that although the model used is only second order, the values of capacitor voltages are close to the V_{cref} and do not drift. Fig. 4.10 (b) shows chopper current and the voltage ripples $v_{c1} - V_{cref}$ and $v_{c2} - V_{cref}$. The waveforms of source voltage v_{sa} (scaled by a factor of 20) and compensated source current i_{sa} show unity power factor relationship in Fig 4.11 (a). It is seen from the figure 4.11 (b) that the compensated source currents are balanced and sinusoidal.



(a) (b)

Fig. 4.11 (a) Source voltage (×20) and source in phase-*a* (b) Three-phase compensated source currents

The reference currents of the compensator are generated as per (3.2). The waveforms of the reference current (i^*_{fa}) and the actual current (i_{fa}) for the compensator, as generated by the action of hysteresis controller, are shown in Fig. 4.12. It can be seen that the compensator tracks the reference current faithfully within the hysteresis band.

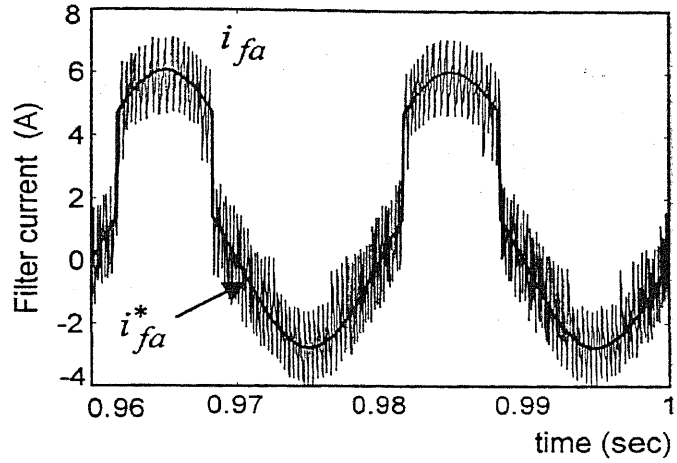


Fig. 4.12 Reference and actual filter current in phase-*a*

The waveform neutral current i_o is shown in Fig. 4.13. It can be seen from this figure that i_o has an oscillating component and an average value of 3.3 amps for the load configuration considered here. The chopper, when activated, compensates for this current. This fact is evident from this figure as both the currents have an average close to 3.3 amps and are of opposite polarity.

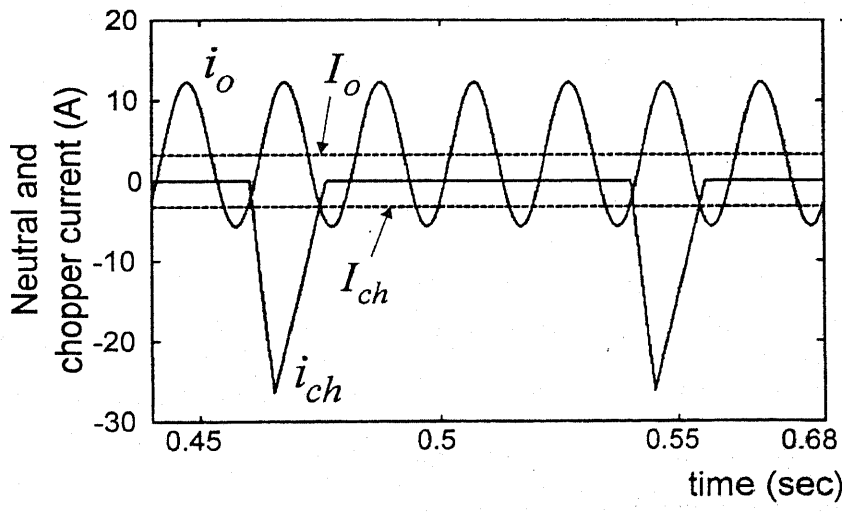


Fig. 4.13 Waveforms of chopper and neutral current

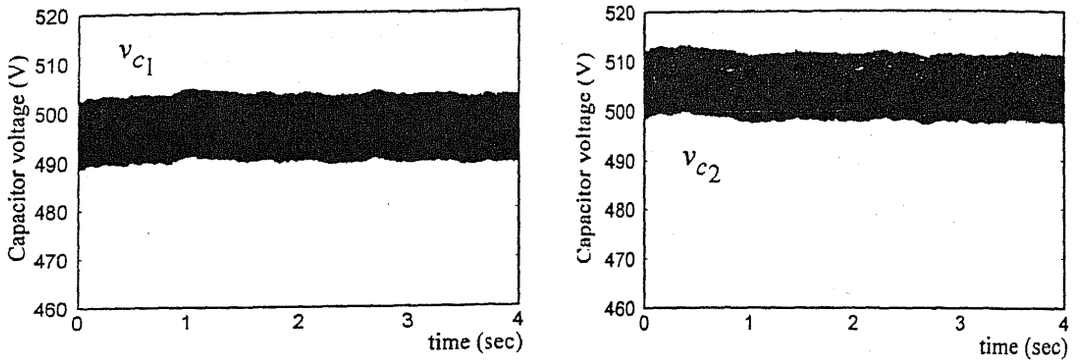


Fig. 4.14 (a) Voltage of capacitor C_1 (b) Voltage of capacitor C_2 when load does not contain dc

Fig. 4.14 (a)-(b) shows the dc capacitor voltages when the half bridge diode rectifier is excluded from the load and the compensator is run without chopper circuit. It can be seen that the voltage imbalance problem does not arise here. However, it is to be noted that even if the dc component forms a very small fraction of the total load, it will cause voltage imbalance in capacitors over several cycles. In this situation, the control circuit activates the chopper for short time to balance the voltages. The chopper remains inactive for a long duration in between. However, the method has disadvantages that the procedure for obtaining the on time of the chopper is computation intensive and it requires a chopper of large current rating.

4.6.2 Single Pulse Control Using Energy Balance

In the above, the on time of the chopper has been computed using the state space model and by solving it through nonlinear equation solver in MATLAB. Even in this case, there is an approximation that the currents i_1 and i_2 in Fig 4.4 are ignored due to fast action of chopper. With this assumption and also neglecting the resistance of the chopper inductor, we can compute on time of the chopper as follows.

Let v_{c1}^{cyl} and v_{c2}^{cyl} be the voltages of capacitors C_1 and C_2 at the end of a cycle of the system voltage in phase-*a*. Suppose the neutral current contains only positive dc

component. As a result, v_{c1} decreases and v_{c2} increases. The extra energy stored in C_2 is given as

$$E_{c_2} = \frac{1}{2}C(v_{c2}^{cyl})^2 - \frac{1}{2}C(V_{cref})^2 \tag{4.24}$$

Now the switch S_8 is closed (Fig. 4.2) till chopper current builds up (Fig. 4.8) so that all extra energy stored in C_2 is transformed to inductor L_{ch}. Therefore the maximum chopper current $i_{ch\max}$ has the following relations

$$\frac{1}{2}L_{ch}\, i_{ch\max}^2 = \frac{1}{2}C\left\{\left(v_{c2}^{cyl}\right)^2 - V_{c\,ref}^2\right\} \tag{4.25}$$

The above equation implies that

$$i_{ch\max} = \sqrt{\frac{C}{L_{ch}}}\left\{\left(v_{c2}^{cyl}\right)^2 - V_{c\,ref}^2\right\}^{1/2} \tag{4.26}$$

The rate of rise of current in chopper inductor is approximately equal to $V_{c\,ref} / L_{ch}$. Therefore,

$$\frac{i_{ch\,max}}{t_{8\,on}} \approx V_{c\,ref} / L_{ch} \tag{4.27}$$

The on time for switch S_8 is then given by,

$$t_{8\,on} = \left\{\left(\frac{v_{c2}^{cyl}}{V_{c\,ref}}\right)^2 - 1\right\}^{1/2} (L_{ch}\, C)^{1/2} \tag{4.28}$$

Similarly, due to negative dc component in neutral current v_{c2} decreases and v_{c1} increases, the approximate on time for switch S_7 is given as,

$$t_{7\,on} = \left\{ \left(\frac{v_{c1}^{cyl}}{V_{c\,ref}} \right)^2 - 1 \right\}^{1/2} (L_{ch} C)^{1/2} \tag{4.29}$$

The above computations are based on energy balance. Using (4.28) and (4.29), we can compute on time for chopper switches S_8 and S_7.

The simulation results with the above strategy are shown in Fig. 4.15. The capacitor voltages are regulated within the voltage band 500±40 V. At instant $t = S_{8\,on}$, the switch S_8 is switched on as v_{c2} is larger than 540 V. As a consequence the chopper brings the v_{c2} near to $V_{c\,ref}$. At instant $t = S_{8\,off}$, S_8 is switched off. The voltage v_{c1} starts rising towards $V_{c\,ref}$ till chopper current reaches zero. For the given load configuration, it takes about 3 cycles for v_{c2} to rise above 540 V and the maximum chopper current is 24 A. The chopper action is complete in less than one cycle. It is also seen from the figure that the average of chopper current is about –3.3 A, which is equal and opposite to the average of load neutral current. However, the single pulse control requires chopper of rating of I_{L_1} or higher (Fig. 4.8). The compensated currents are similar to those shown in Fig. 4.11 (a) and (b).

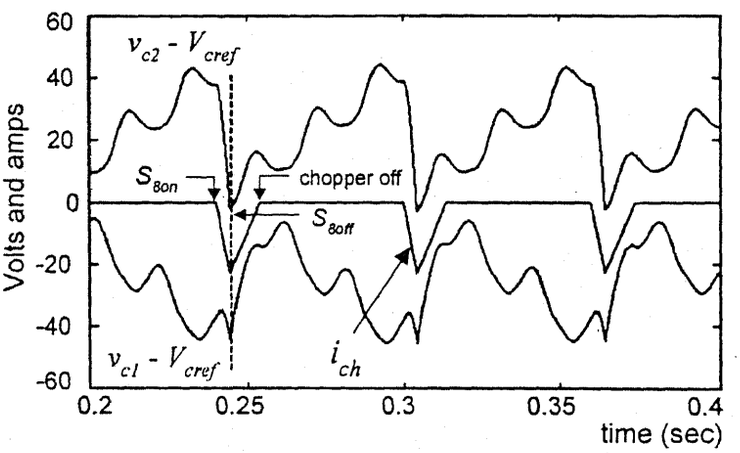


Fig. 4.15 Voltage ripples and chopper current in single pulse control

4.6.3 Multi Pulse Control of Chopper

In single pulse control, the chopper current rating may be large due to high value of $i_{ch\,max}$ as per (4.26). A reduction in the chopper current rating is possible if the chopper is operated with a current limit, $I_{ch\,limit}$, which is a fraction of $i_{ch\,max}$. However this requires a number of pulses of chopper operation to reduce the capacitor voltage imbalance. The corresponding ideal state trajectories for capacitor voltages and chopper current are shown in Fig. 4.16. In this figure, Δv_c is a limit on either side of $V_{c\,ref}$ within which capacitor voltages are regulated [59].

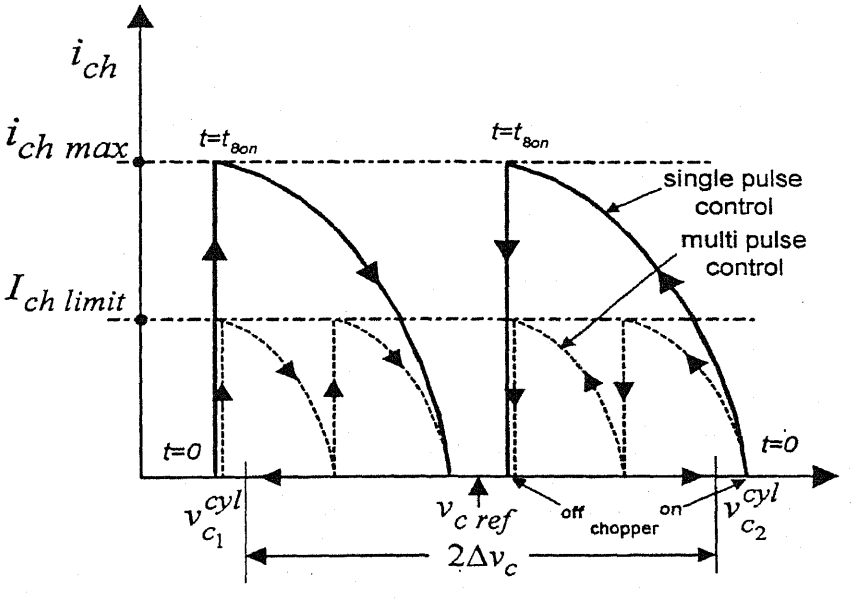


Fig. 4.16 Ideal state trajectories of capacitor voltages and chopper current

In this strategy, the on time of the chopper switches is not computed. Instead, the switch S_7 or S_8 is closed depending upon the result of comparison of the larger of v_{c1}^{cyl} and v_{c2}^{cyl} with the voltage limit ($V_{c\,ref} + \Delta v_c$). The switch is kept closed till the chopper current i_{ch} reaches the pre-defined current limit, $I_{ch\,limit}$. The switch is kept open till i_{ch} is reduced to zero. The capacitor voltage under consideration is sampled and compared with $V_{c\,ref}$. If it is larger than $V_{c\,ref}$, the chopper cycle is repeated. The process is continued till the

capacitor voltage is close to $V_{c\,ref}$. The chopper current consists of a number of consecutive current pulses, each of which is similar to that shown in Fig. 4.8. In this method, the chopper current is limited to $I_{ch\,limit}$ which is less than $i_{ch\,max}$. The ideal state trajectories for multi pulse operation are shown by dotted lines in Fig. 4.16.

A block diagram for the chopper with multi pulse control is shown in Fig. 4.17. The block diagram is also applicable to single pulse control, where the inputs i_{ch} and $I_{ch\,limit}$ may be ignored.

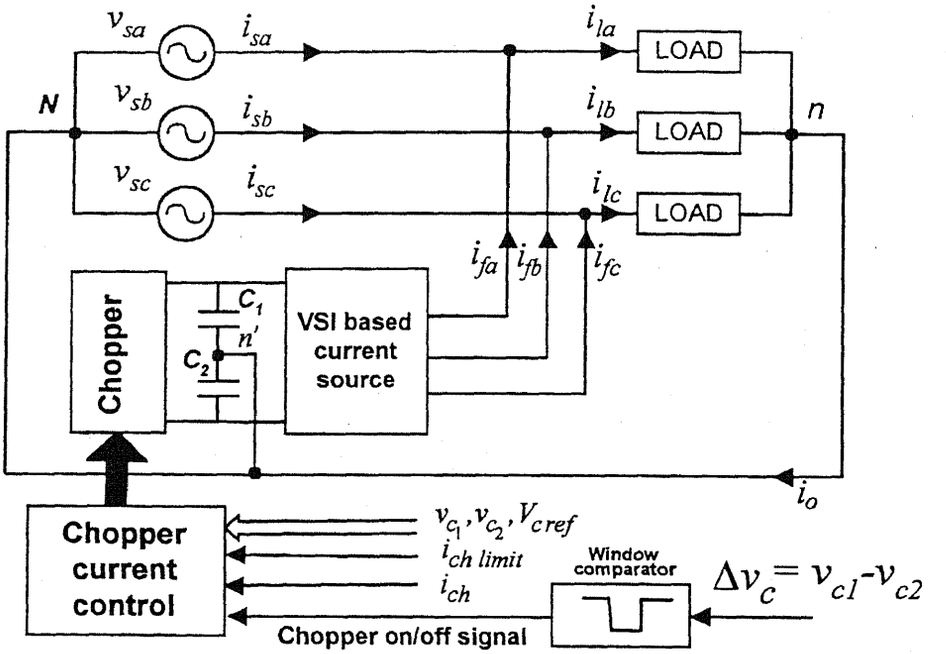


Fig. 4.17 General block diagram for multi pulse chopper control

In the simulation of single pulse control, the maximum chopper current reaches 24 A (Fig. 4.15). If the current rating of the chopper is to be reduced, multi pulse control with current limit may be employed. In this simulation, we set a current limit of 15 A for the chopper for the capacitor voltage limits of 500 ± 40 V. The capacitor voltage ripples and the chopper currents are shown in Fig. 4.18.

At point t_8, v_{c2} is above 540 V, hence the chopper is activated. The switch S_8 is opened and closed repeatedly with a current limit of 15 A, till voltages of the capacitors are

close to V_{cref}. This is achieved at point t_8'. Therefore at point t_8' the chopper is turned off. The chopper remains off till v_{c2} again crosses the limit of 540 V, and the chopper operation is repeated. Thus, with slower response, the chopper with reduced current rating can be used for capacitor voltage equalization.

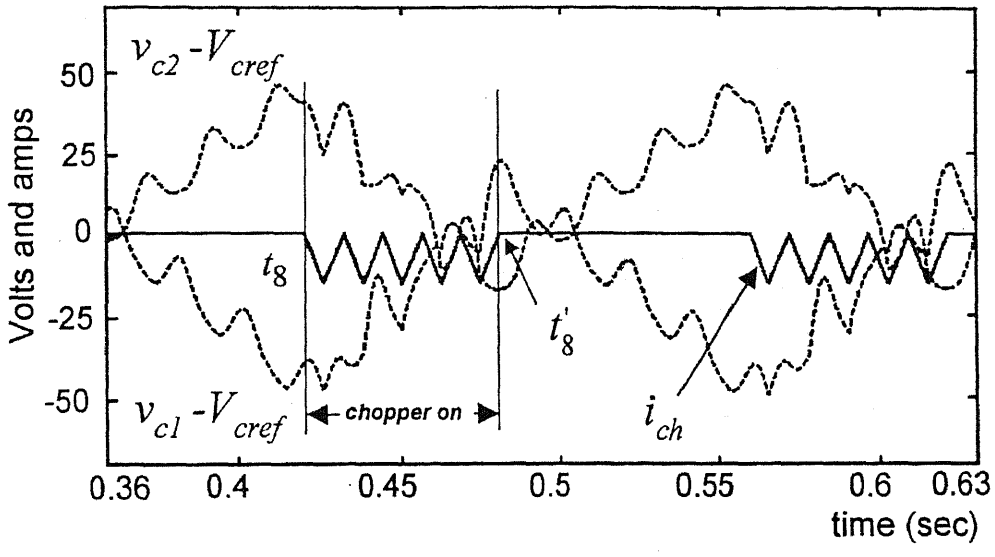


Fig. 4.18 Voltage ripples and chopper current in multi pulse control

4.6.4. Open Loop Duty Cycle Control

In this control scheme, the chopper current is not sensed. Instead, neutral current i_o in the path $n-n'$ (Fig. 4.1) is sensed. The negative of average neutral current $-I_o$ is generated with an operational amplifier low pass filter. In the steady state the chopper is operated in Discontinuous Conduction Mode. The limiting value of duty cycle (D) is 0.5 as shown in Fig. 4.19.

In reference to Fig. 4.19, let s be the slope of chopper current. The value of s depends upon the capacitor voltages, R_{ch} and L_{ch}. It is generally varying over small range as v_{c1} and v_{c2} are also varying. However, its value can be taken as a constant for all practical purposes. In Fig. 4.19, T refers to the time period of chopper operation and D is the duty cycle. Considering i_o with positive dc component, v_{c1} decreases and v_{c2} increases. To regulate the voltages of the two capacitors switch S_8, (Fig. 4.4), is to be operated at a

certain duty cycle for a given dc component in the neutral. The duty cycle (D) of switch S_7 or S_8 is computed as discussed below.

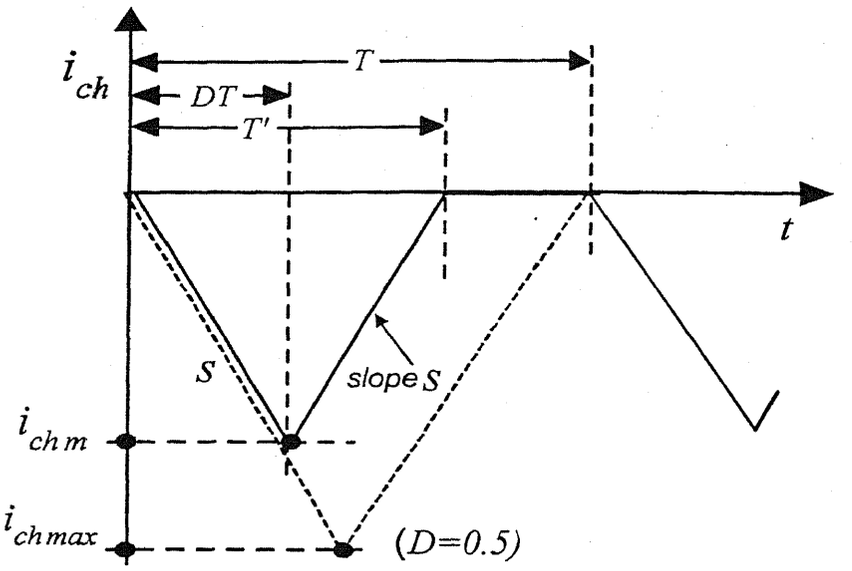


Fig. 4.19 Open loop duty cycle control

The magnetic energy in chopper inductor is released at almost the same voltage level at which it was stored when S_8 was closed. Therefore, the positive and negative slopes of chopper current can be taken as equal. Thus in Fig. 4.19,

$$T' = 2DT \tag{4.30}$$

Let us choose a current $i_{ch\,m} < i_{ch\,max}$. From Fig. 4.19, it is given by

$$i_{ch\,m} = \frac{V_{c\,ref}}{L_{ch}} DT \tag{4.31}$$

The average chopper current generated should be equal to the average load current. Therefore,

$$\frac{1}{2} \frac{i_{ch\,m}\, T'}{T} = I_o \tag{4.32}$$

Substituting T' and i_{chm} from (4.30) and (4.31) in (4.32), we get

$$D = k\sqrt{I_o} \tag{4.33}$$

where $k = \sqrt{\frac{L_{ch} f}{V_{c\,ref}}}$, $f = 1/T$ being the chopper frequency.

In (4.33), the I_o is always positive. However the polarity of I_o determines which chopper switch is to be operated. For positive (negative) I_o, S_8 (S_7) is operated. Equation (4.33) gives the control law for duty cycle based on the measurement of i_o and its averaging. The above derivation neglects the deviations of v_{c1} and v_{c2} from $V_{c\,ref}$. In practice, such deviations may exist. Therefore, (4.33) is modified by feedback of $\Delta v_c = v_{c1} - v_{c2}$ as

$$D = k\sqrt{I_o - k_v \Delta v_c} \tag{4.34}$$

where k_v is a positive voltage gain. If I_o is positive and initial Δv_c is negative, then D is increased in order to overcome this initial voltage imbalance. The block diagram of this scheme is shown in Fig. 4.20. The low pass filter allows only the dc component of i_o.

It is to be noted that the in steady state, $\Delta v_c \to 0$. The maximum value of D is 0.5. Therefore, the limit of the maximum average neutral current that can be compensated is $1/4k^2$ which equals $V_{c\,ref}/4L_{ch} f$. For larger value of I_o the chopper may enter into continuous conduction mode. In such a case, other proposed control strategies in Section 4.7 may be preferred.

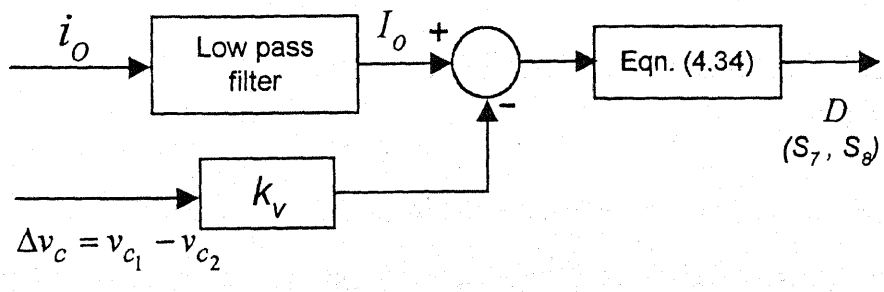
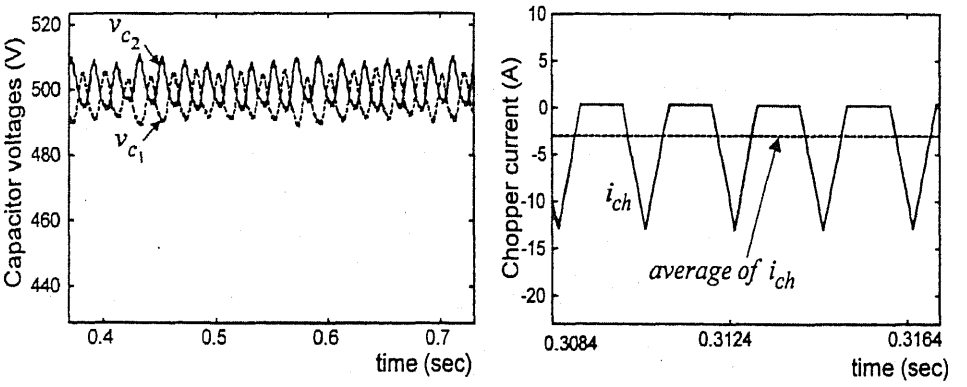


Fig. 4.20 Block diagram for loop duty cycle control

In this strategy, for the load currents given in Fig. 4.5, the duty cycle is determined using (4.34). The upper limit of chopper frequency is decided by the switching losses in the chopper and its inductor L_{ch}. The chopper switching frequency of 500 Hz is chosen in the simulation. For given parameters, the duty cycle of the chopper switch using (4.34) is 25%. This switching frequency and duty cycle are also seen in Fig. 4.21 (b). Since i_o has positive dc component, switch S_8 is operated at frequency of 500 Hz with 25% duty cycle.

The steady state capacitor voltages and chopper currents are shown in Fig. 4.21 (a) and (b). It is seen from Fig. 4.21 (a) that the capacitor voltages are regulated close to reference value. Fig. 4.21 (b) confirms that the average chopper current (-3.3 A) is approximately equal to the negative of average of i_o. It indicates that the chopper nullifies the effect of dc component of current in the load as desired. Due to feedback of Δv_c the drift in capacitor voltages is absent. The small ripples in voltages are due to ac component of the neutral current. The compensated source current waveforms are similar to as shown in Fig. 4.11 (a) and (b).



(a) (b)

Fig. 4.21 (a) Capacitor voltages (b) Chopper current using open loop duty cycle control

4.7 OUTER VOLTAGE AND INNER CURRENT LOOP CONTROL SCHEMES

In single pulse control scheme, we use an approximation in which the currents i_1 and i_2 (Fig. 4.4) are ignored due to fast action of chopper. However, this method has the disadvantage that the peak chopper current is large. Not only that, if there is initial voltage

imbalance in capacitors, the chopper current may shoot up to a high value which may damage the IGBT switch. To overcome this problem, a control scheme using outer voltage and inner current loop is proposed. This control scheme has faster dynamics due to inclusion of chopper current feedback. Two schemes, PI duty cycle control and hysteresis control schemes have been described.

The general block diagram is shown in Fig. 4.22. The current i_o in the load neutral path $n-n'$ is sensed and filtered out to remove the fundamental and the harmonics thus leaving only I_o (the average value of i_o). The difference in capacitor voltages, $v_{c1}-v_{c2}$ is sensed and filtered out to remove the ripples. The filtered output voltage is denoted as $\Delta V_c = V_{c1} - V_{c2}$. The proportional voltage controller outputs a control signal, $k_v \Delta V_c$, which is added to $-I_o$ to generate the reference chopper current, i_{ch}^*. The inner control loop ensures that the average chopper current is equal to i_{ch}^*. The current loop has faster dynamics than the voltage control loop [60].

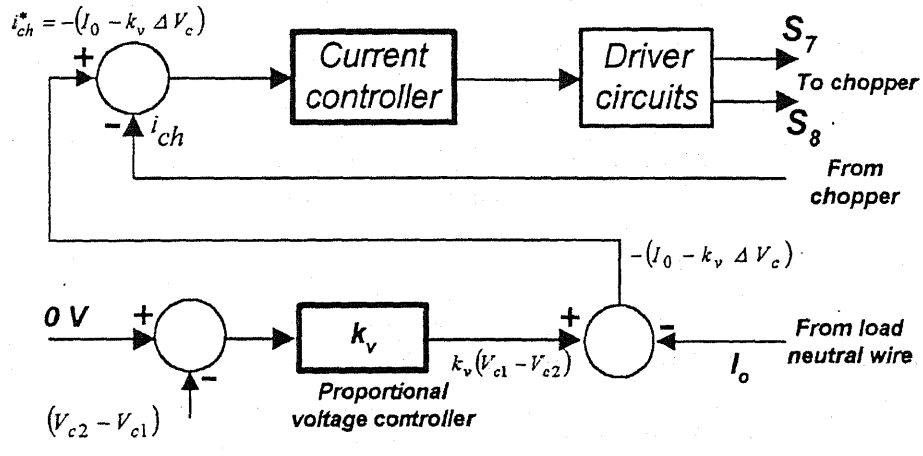


Fig. 4.22 Schematic of outer voltage and inner current control of chopper

The reference current for chopper can be written as

$$i_{ch}^* = -(I_o - k_v \Delta V_c) \tag{4.35}$$

An error e_i is formed using reference chopper current as per (4.35) and actual chopper current i_{ch}

$$e_i = i_{ch}^* - i_{ch} \tag{4.36}$$

The current controller of Fig. 4.22 can be a hysteresis controller or a PI controller. In the following sub-sections, these two chopper control schemes to equalize the voltages of the capacitors have been discussed.

4.7.1 PI Duty Cycle Control

In this method, the chopper is run at fixed frequency, which is sufficiently high so that i_{ch} smoothly tracks i_{ch}^*. The current controller in Fig. 4.20 is a PI controller. The duty cycle is limited between 0 and D_{max} and is determined as follows.

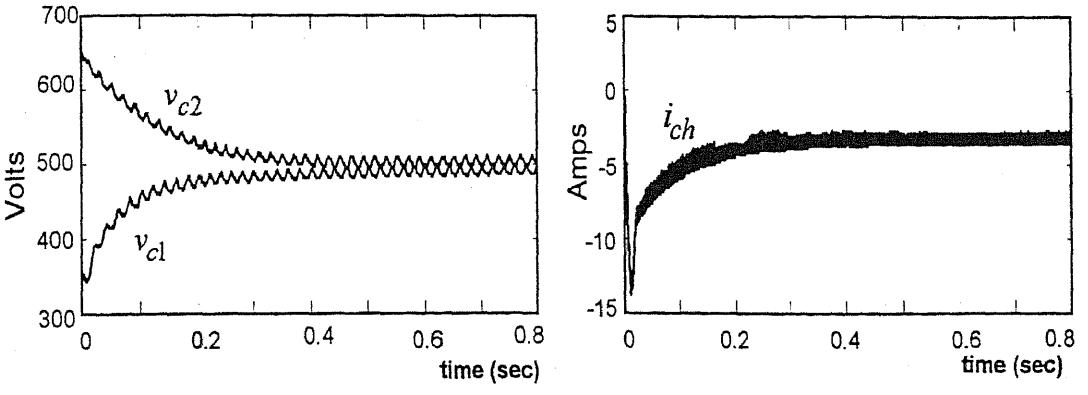
$$D = K_{cp}\, e_i + K_{ci} \int e_i\, dt \tag{4.37}$$

where, K_{cp} and K_{ci} are proportional and integral constants of the PI controller for chopper duty cycle control. The steady state value of D is approximately 0.5 for a high Q inductor. The value of D_{max} is always chosen to be higher than 0.5. Its value decides the maximum chopper current and the transient response of the loop. Its is chosen to be 0.7 in the simulation.

Depending upon the polarity of ΔV_c, a particular switch of chopper, S_7 or S_8, is operated. If ΔV_c is less than or equal to zero, then switch S_8 is operated at duty cycle given by (4.37). If ΔV_c is greater than zero, then switch S_7 is operated at duty cycle given by (4.28).

In the simulation, the chopper is operated at a frequency of 1800 Hz. The chopper current i_{ch} computed from the state space model (4.7) and using (4.35)-(4.37), the duty cycle D is calculated. The capacitor voltages and chopper currents are shown in Fig, 4.23 (a) and 4.23 (b) respectively. An initial voltage imbalance of ± 150 V is considered. From Fig. 4.23 (a) it is seen that the chopper is able to cancel the initial voltage imbalance and

maintain the capacitor voltages at the reference value of 500 V. As a result the compensator is able to work satisfactorily.



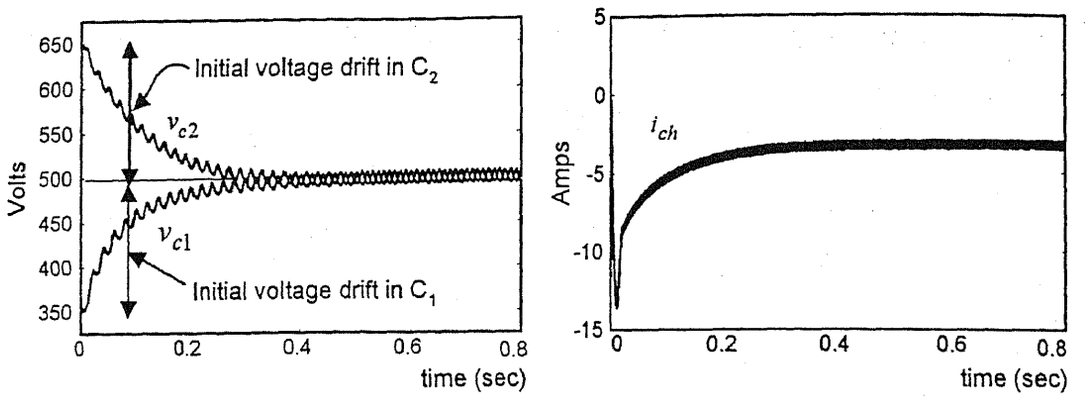
(a) (b)

Fig. 4.23 (a) Capacitor voltages (b) Chopper current with duty cycle control

4.7.2 Chopper Control in Hysteresis Band Current Control

In this control scheme, the chopper circuit is employed to track i_{ch}^{*} in a hysteresis band. The block diagram is same as given in Fig. 4.22 where current controller is a hysteresis controller. This control scheme nullifies the initial voltage imbalance in capacitors as well as the voltage drift due to dc component of the load current. As compared to the single pulse control, this method has the advantage that i_{ch} is limited to $-I_o$ in the steady state. In case of single pulse control, i_{ch} may reach a value, which is 3 or 4 times that of I_o and thus the switching devices and inductors need to be over-rated.

In this control scheme, the switches S_7 and S_8 are controlled in such a way that the chopper circuit tracks $-(I_o - k_v \Delta V_c)$. This counteracts the initial voltage imbalance in the capacitors and nullifies the effect of I_o on capacitor voltages in the steady state. The simulation results are shown in Fig. 4.24 (a) and (b). From Fig. 4.24 (a), it is seen that with hysteresis controller both the voltages v_{c_1} and v_{c_2} are stabilized to the reference value of 500 V with small ripple. In Fig. 4.24 (b), the chopper current i_{ch} which is tracking the reference value $-(I_o - k_v \Delta V_c)$ with a hysteresis band of ± 0.2 A, is shown. For this hysteresis band, the chopper switching frequency is approximately 3 kHz in steady state.



(a) (b)

Fig. 4.24 (a) Capacitor voltages (b) Chopper current with hysteresis band current control

In hysteresis band control mode, the switches S_7 and S_8 (Fig. 4.1) are operated at high frequency. Therefore, the switching losses in hysteresis control associated with these switches are higher than that in PI duty cycle control.

4.7.3 Current Rating of the Chopper

If the frequency of chopper is sufficiently high such that i_{ch} is nearly ripple free, then chopper current rating is at least $i_{o\max}$. An additional current rating is required to provide the component, $k_v \Delta V_c$, of the chopper current to correct any initial voltage unbalance at the time when chopper starts working. Under dc load condition, when chopper is not turned on, one of capacitor voltage settles around peak of system phase voltage, v_{peak}. The other capacitor will have a voltage of $2V_{cref} - v_{peak}$. Therefore in the worst case, the current rating of the chopper should be approximately $2k_v\left(V_{cref} - v_{peak}\right) + i_{o\max}$. For example, in simulation, $V_{c\,ref} = 500$ V and $v_{peak} = 360$ V. For $k_v = 0.02$, the current rating of the chopper is found to be approximately 18 amps. It is seen from the simulation result of Fig. 4.23 (b) and 4.24 (b) that the peak chopper current is 14 A, which compares well with the worst case value calculated above.

4.8 EXPERIMENTAL RESULTS

In this section experimental results for chopper operation with hysteresis control scheme of Sub-section 4.7.2 and open loop control of Sub-section 4.4 are given. A scaled down prototype with voltages reduced by a factor of 10 has been chosen for experimentation. The source voltages are balanced and sinusoidal with a peak of 36 volts. Thus for the same load parameters as given in Table 4.1, the currents are also reduced by a factor of 10. The system voltages v_{sa}, v_{sb}, v_{sc} and load current i_{la}, i_{lb}, i_{lc} are sensed using Hall effect voltage and current transducers. The voltage and current signals are acquired by PC (P-II, 350 MHz) through data acquisition card (9118 DG NuDAQ). The algorithm for reference filter currents is implemented in C language. To obtain the average load power ($\bar{p}_l$), moving average filter has been used. Then, filter reference currents are generated using (3.2).

The steady state load currents are shown in Fig. 4.25. As seen from Fig. 4.25, the load currents are unbalanced ac due to unequal resistive loads of 26 Ω, 35 Ω and 100 Ω, in phases *a*, *b* and *c* respectively. In addition, there is a dc output current of 0.33 A due to three-phase half wave rectifier. The total dc component of the neutral current I_o shown by dotted line in Fig. 4.25, is 0.33 A.

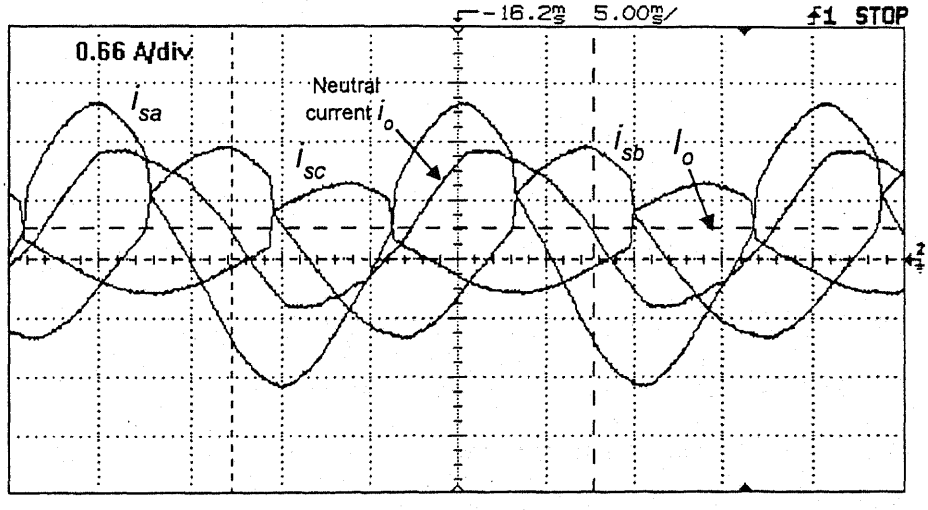


Fig. 4.25 Experimental load currents

4.8.1 Operation without Chopper

Initially the load is unbalanced resistors only and therefore the voltages of the capacitors C_1 and C_2 are regulated to 50 volts, which is above the peak system voltage of 36 volts. The rectifier containing dc is switched on at instant t_1 as shown in Fig. 4.26. Due to the action of dc component of neutral current I_o, the capacitor C_1 is discharged, while capacitor C_2 is charged till v_{c1} settles at a little below the peak of the system voltage (approximately 25 V). However the PI voltage control loop of inverter with gains $K_p = 0.3$, $K_i = 0.001$ maintains the total capacitor voltage $(v_{c1} + v_{c2})$ at 100 volts. The tracking current performance of the compensator in phase-a is shown in Fig. 4.27. It is seen in Fig. 4.27, that the tracking is lost between point p and q, because v_{c1} is close to system voltage v_{sa}. Between points r and s the slope of i_{fa} is negative due to the fact that v_{c1} is little below than v_{sa}. These experimental results are similar to the simulation results given in Fig. 4.7.

4.8.2 Operation with Chopper: Hysteresis Control

In this experiment, the compensator is operated first without chopper as discussed above. The chopper is then turned on and operated using hysteresis band current control, which is tracking $-(I_o - k_v \Delta V_c)$. The active low pass filters with cut off frequency of 10 Hz are used to obtain I_o from the signal i_o and ΔV_c from v_{c1} and v_{c2}. In experiment, the value of k_v is chosen 0.001. In the steady state, ΔV_c tends to be zero and the chopper effectively tracks $-I_o$ to keep the voltages of the dc capacitors close to the reference value. This situation is shown in Fig. 4.28, displaying the waveforms of $-I_o$ and i_{ch}. It is also seen in Fig. 4.28 that the switching frequency of chopper, as observed from waveform of i_{ch} is approximately 500 Hz. This relatively low switching frequency is due to the large hysteresis band and chopper inductor L_{ch}, which is taken as 40 mH.

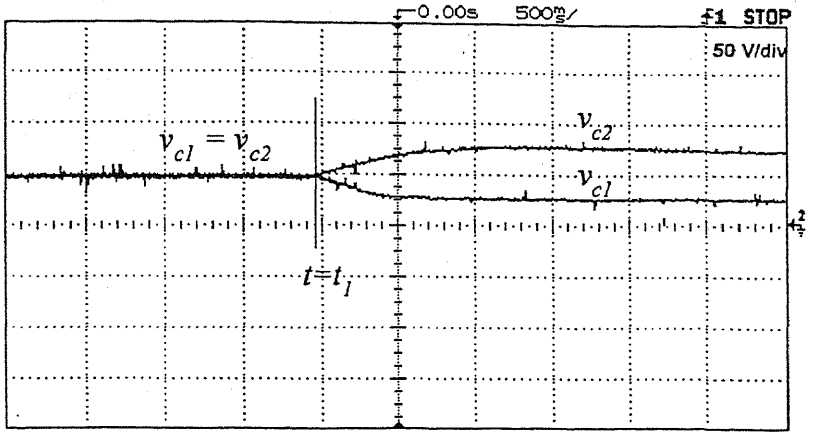


Fig. 4.26 Voltage imbalance in capacitors: Experimental

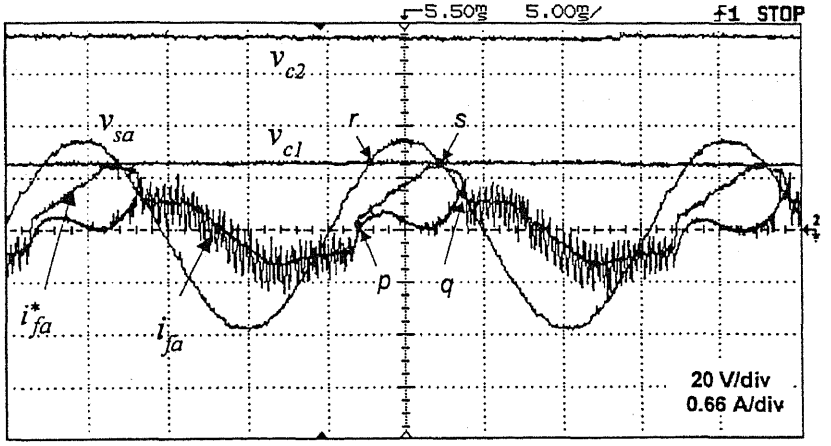


Fig. 4.27 Effect of dc load on tracking performance: Experimental

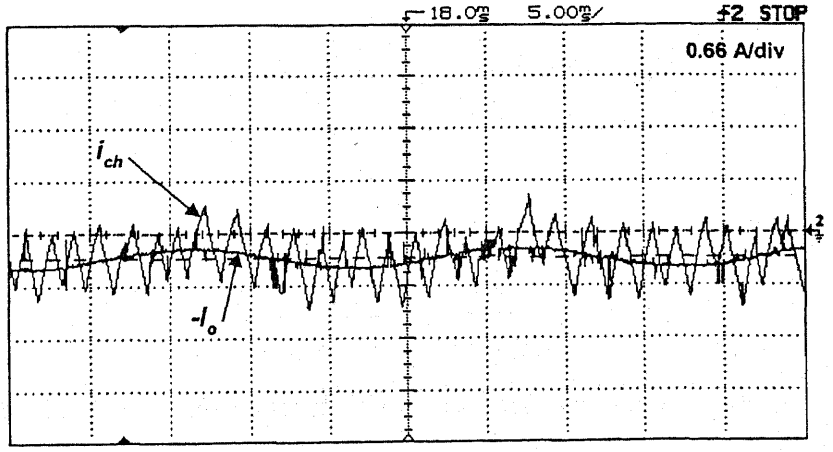


Fig.4.28 Chopper current using hysteresis control

Fig. 4.29 shows that the capacitor voltages v_{c_1} and v_{c_2} are equalized, close to the reference value of 50 V each due to chopper action. This ensures a good tracking performance of the inverter. The resulting compensated source currents are shown in Fig. 4.30. It is seen that the source currents after compensation are balanced and sinusoidal and are in phase with their respective phase voltages. The chopper is thus able to nullify the effect of dc component of the neutral current in the steady state.

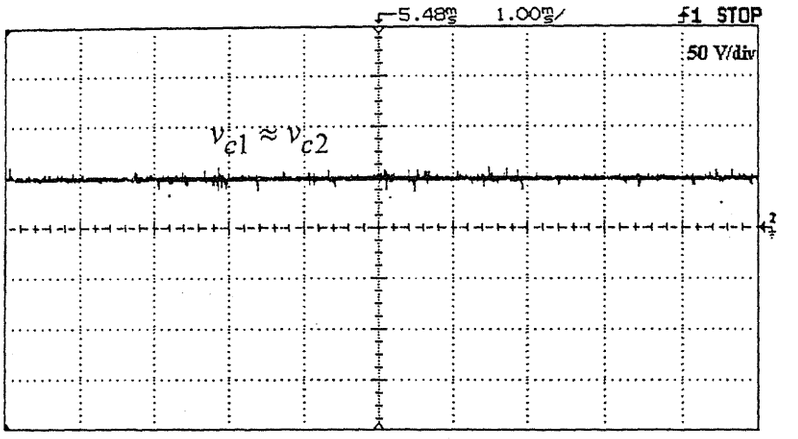


Fig. 4.29 Equalized voltage due to chopper action

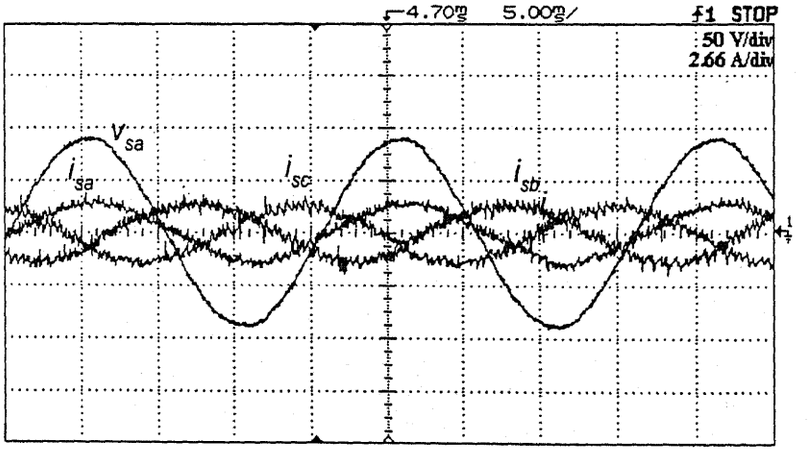


Fig. 4.30 Compensated source currents

4.8.3 Operation with Chopper: Open Loop Duty Cycle Control

For open loop duty cycle control described in Sub-section 4.6.4, the chopper current is shown in Fig. 4.31. It is seen from Fig. 4.31, that the duty cycle of chopper is approximately is 25%. The peak value of chopper current is 1.4 A. Therefore, using (4.32), average value of chopper current is - 0.35, which is very close to I_o, whose value is 0.33 A. It should be noted that chopper inductor L_{ch} for open loop duty cycle control is taken as 0.02 H. The negative of average neutral current is computed by active low pass filter with cut off frequency of 10 Hz in the experiment. The capacitor voltages are regulated close to reference value i.e. 500 V. The waveforms of capacitors voltages are similar to as shown in Fig. 4.29. The compensated source currents are sinusoidal and balanced. Their waveforms are similar to as shown in Fig. 4.30.

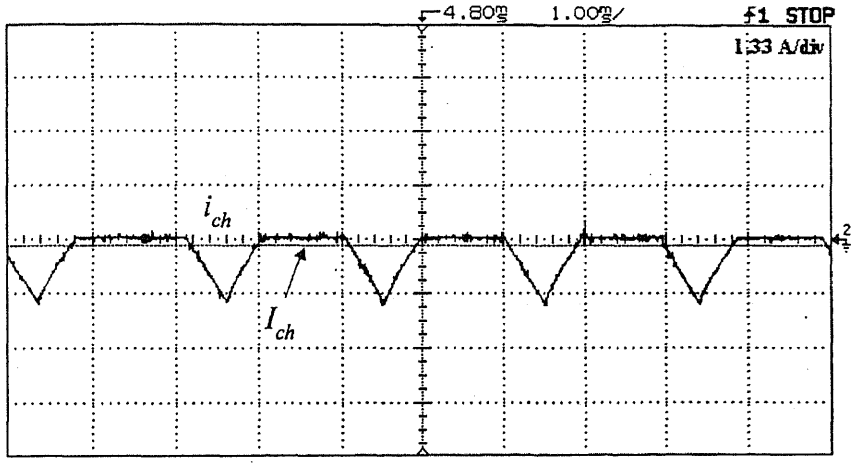


Fig. 4.31 Chopper current using open loop duty cycle control

4.9 CONCLUSIONS

A shunt compensator topology with two dc storage capacitors and a three-phase voltage source inverter is proposed for three-phase, four-wire distribution systems. It is capable of compensating sinusoidal or non-sinusoidal load currents that may also contain dc. A detailed state space model of the compensator is derived. The problem of voltage imbalance in case of loads containing dc component in line currents is discussed in detail. It has been shown that voltage imbalance in dc capacitors results in degraded performance of the

compensator. To ensure the correct performance of the compensator, the voltage of the capacitors should be regulated to the reference value.

A two-quadrant chopper circuit is employed along with the compensator to regulate the voltage of the capacitors. Six different control schemes namely, (i) Single pulse control using state space model (ii) Single pulse control using energy balance method (iii) Multi pulse control (iv) Open loop duty cycle control (v) PI duty cycle control and (vi) Hysteresis control have been proposed. For each of these control schemes the detailed simulation results are presented. It has been demonstrated that the control schemes are able to stabilize the voltages of the capacitors close to the reference value. This ensures the correct performance of the compensator. The hysteresis control and open loop duty cycle control schemes have also been verified through the experimental results.

CHAPTER 5

LOAD COMPENSATION WITH NON-STIFF SOURCE

In the previous chapters, we have proposed the various load compensation schemes, that assume the source at the point of common coupling (PCC) to be stiff. In practice however, the load is remote from a distribution substation and is supplied by a feeder. The switching frequency harmonic components generated by the inverter distort both the voltages at the PCC and the source current. The compensation algorithms presented in Chapter 2 require the measurements of the PCC voltages. Thus if the voltages are distorted due to switching frequency harmonics, the reference currents generated by the compensation algorithm will also be distorted. Thus a straightforward application of the algorithm can result in poor compensation.

In this chapter we shall discuss the load compensation problem assuming the 'upstream' source to be non-stiff. To bypass the inverter switching frequency harmonic components a filter capacitor is connected in parallel with the compensator at PCC. However, the presence of the capacitor causes problem as it changes the dynamics of the compensating system. A hysteresis based current controller can not be used now for this purpose. Instead a state feedback tracking controller is used. The design of the state feedback controller requires careful considerations like choice of gain matrix, robustness properties and reference current generation. In this chapter, we shall discuss all the above aspects.

5.1 COMPENSATOR PERFORMANCE WITH NONSTIFF SOURCE

In general, there may be various feeder segments and load buses before the PCC. At the best, the source and the feeder impedance are the Thevenin equivalent obtained by looking into the network at PCC. Thus, not only is the feeder impedance not known 'a priori', it may change suddenly depending on the loads that are connected at the 'upstream' buses. A non-stiff source supplying loads is shown in Fig. 5.1.

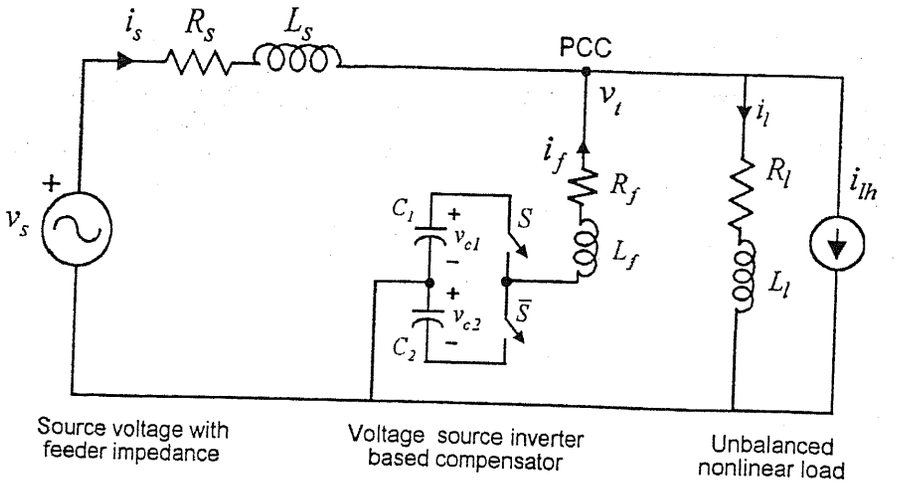


Fig. 5.1 Single line diagram of shunt compensation of a load with non-stiff source

Let us denote the feeder resistance and inductance (Thevenin equivalent of system) as R_s and L_s respectively. Then the voltage at the point of common coupling is

$$v_t = v_s - i_s R_s - L_s \frac{di_s}{dt} \tag{5.1}$$

Since the PCC is the terminal at which the compensator is connected, we thus denote this voltage as the terminal voltage.

Equation (5.1) clearly shows that if the source current is distorted, the voltage at the PCC also gets distorted. Since this voltage is used in compensation algorithm, it results in further distortion of the source current. To illustrate the idea let us choose the following parameters:

Table 5.1 System parameters

System Parameters	**Values**
System voltage	360 V peak
Loads	$Z_a = 40 + j\,5\ \Omega$, $Z_b = 50 + j\,5\ \Omega$, $Z_c = 72 + j\,84\ \Omega$.
DC capacitors	$C_1 = C_2 = 2200\ \mu F$, each capacitor held at 500 V dc
Feeder impedance	$Z_s = 1 + j\,3.14\ \Omega$
Interface impedance	$R_f = 1\ \Omega$, $L_f = 40$ mH

It is assumed that the source is balanced and sinusoidal. We now use (3.2) with $P_{loss} = 0$ (as rectifiers supply dc capacitors) and $\gamma = 0$ (unity power factor) for reference current generation. Load currents when compensator is not connected, are shown in Fig. 5.2 (a). The terminal voltages and source currents, when the compensator is switched on at $t = 0.01$ sec are shown in Fig. 5.2 (b) and (c) respectively. It is seen from Fig 5.2 (b) and Fig. 5.2 (c) that both the terminal voltages and source currents contain several high frequency notches and ripples that are attributed to the inverter switching frequency. As a consequence of distortion in the terminal voltage, the load currents also get affected. The load currents after compensation are shown in Fig. 5.2 (d). Clearly these contain high frequency ripples that are not present in the uncompensated waveforms of Fig. 5.2 (a).

The above example clearly shows that unless the switching frequency components of the terminal voltages are eliminated, there will be distortion in the compensated quantities. In order to provide a path for the harmonic component, we connect an ac capacitor in parallel with the compensator at the PCC as shown in Fig. 5.7. Since this capacitor is used for filtering, we call it filter capacitor and denote it by C_f. The performance of this simplistic solution is discussed below.

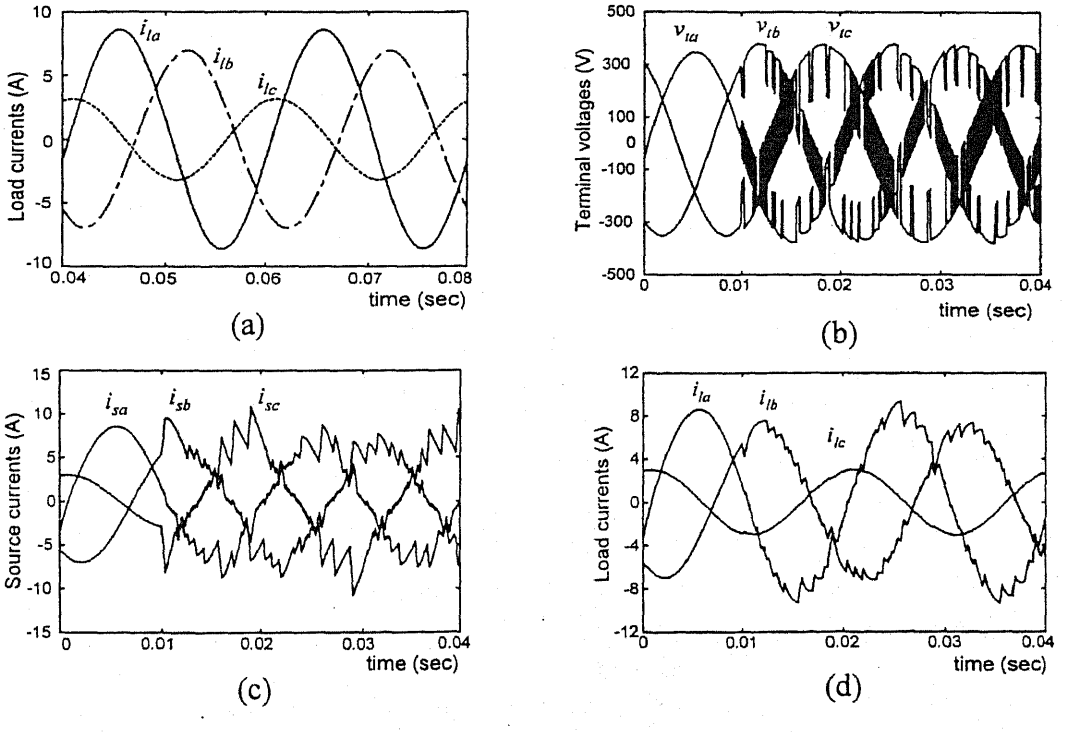
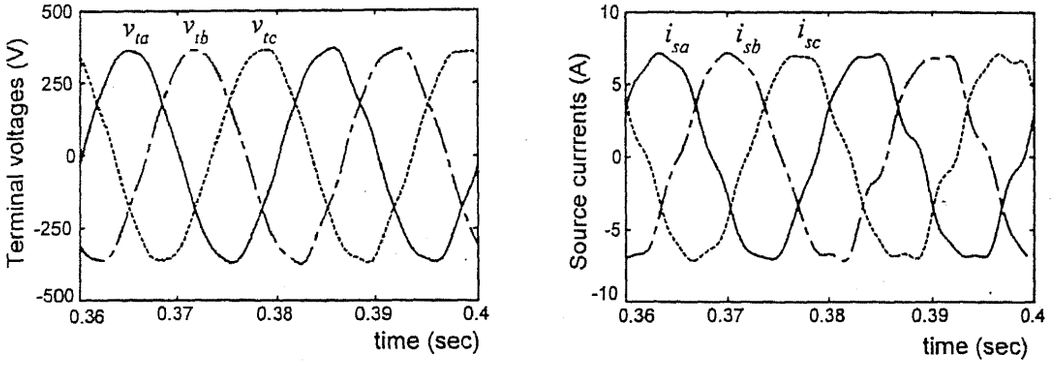


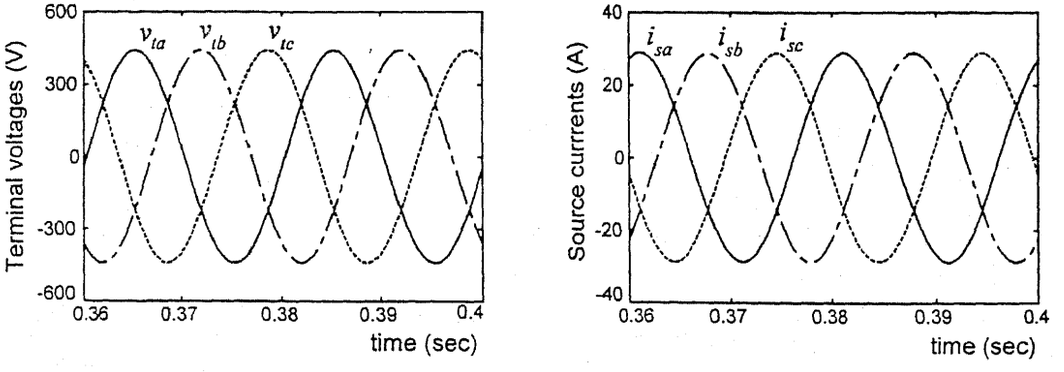
Fig. 5.2 (a) Unbalanced load currents (b) Terminal voltages (c) Source currents (d) Load currents after compensation

No significant advantage can be obtained by such a connection without giving proper consideration to other factors. For example if C_f = 30 μF is connected and the shunt algorithm is implemented, the terminal and source current waveforms are shown in Fig. 5.3 (a) and (b) respectively. The peak values of terminal voltage and source current are 365 V and 7.1 A respectively. Though switching frequency components in these waveforms reduce considerably, the waveforms still remain distorted. The terminal voltage and source current waveforms are shown in Fig. 5.4 (a) and (b) respectively, when C_f is increased to 200 μF. It is seen from these waveforms that there is a significant increase in the magnitude of source currents and voltages (peak values are 29 A and 400 V respectively). The compensator with ac filter capacitor is analyzed in detail in Section 5.3 to explain the above.



(a) (b)

Fig. 5.3 (a) Terminal voltages (b) Source currents with C_f =30 μF



(a) (b)

Fig. 5.4 (a) Terminal voltage (b) Source current in phase a with C_f = 200 μF

5.2 USING SHUNT ALGORITHM WITH POSITIVE SEQUENCE EXTRACTION OF TERMINAL VOLTAGES

From the results of Section 5.1 it is seen that if the terminal voltages are distorted, they can no longer be fed to the shunt algorithm. To improve the performance of the algorithm, we must feed it a balanced three-phase voltage as in the case of a stiff source. We therefore extract the positive sequence components of terminal voltages using the power invariant instantaneous symmetrical transform. This is given by,

$$v_{ta012} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix}$$

where $a = e^{j120^o}$. Let us now define the zero, positive and negative sequence phasors as, V_{ta0}, V_{ta1} and V_{ta2} respectively. Defining a vector as $V^t_{ta012} = \begin{bmatrix} V_{ta0} & V_{ta1} & V_{ta2} \end{bmatrix}$, the following equation is used to obtain the symmetrical components [80].

$$V_{ta012} = \frac{\sqrt{2}}{T} \int_{t_1}^{t_1+T} v_{ta012}\, e^{-j(\omega t - 90^\circ)}\, dt$$

where t_1 is any instant and T is the duration of half of the fundamental period. A mirror image symmetry in v_{ta}, v_{tb}, v_{tc} is assumed. The integral can be computed through a moving average filter.

For the present case, we assume a balanced supply voltage v_s in Fig. 5.1 and as a consequence the terminal voltage will be balanced provided the source current can be balanced. To force this, we feed only the fundamental of the positive sequence into our reference current generation algorithm. Let the voltage phasor be given by $V_{ta1} = \left|V_{ta1}\right| \angle \phi_{ta1}$. Then the instantaneous reference voltage of phase-a will be

$$v_{ta1} = \sqrt{2}\left|V_{ta1}\right| \sin(\omega t + \phi_{ta1})$$

where the time instant is assumed to be phase locked with phase-a terminal (PCC) voltage. The other two phase voltage v_{tbl} and v_{tcl} can be obtained from phase-a voltage v_{tal} by phase shift of -120° and 120° respectively.

These balanced sinusoidal voltages are now fed to the shunt algorithm. As a result of this, the compensated source currents become balanced and sinusoidal. However, they still contain the switching frequency components and so does the terminal voltages. These are shown in Fig. 5.5 (a) and (b) respectively. Now along with the R-L load, three-phase diode bridge is also connected drawing a dc current of 5 A. With this load, phase-a source current and terminal voltage are shown in Fig. 5.6 (a) and (b) respectively. It is seen that the terminal voltage and source current contains the four spikes in each cycle. These are due to switchings of the diode rectifier. These are not desirable and need to be removed. For simulation results in Fig. 5.6 (a) and (b), is chosen 20 mH and hysteresis band 0.4 A.

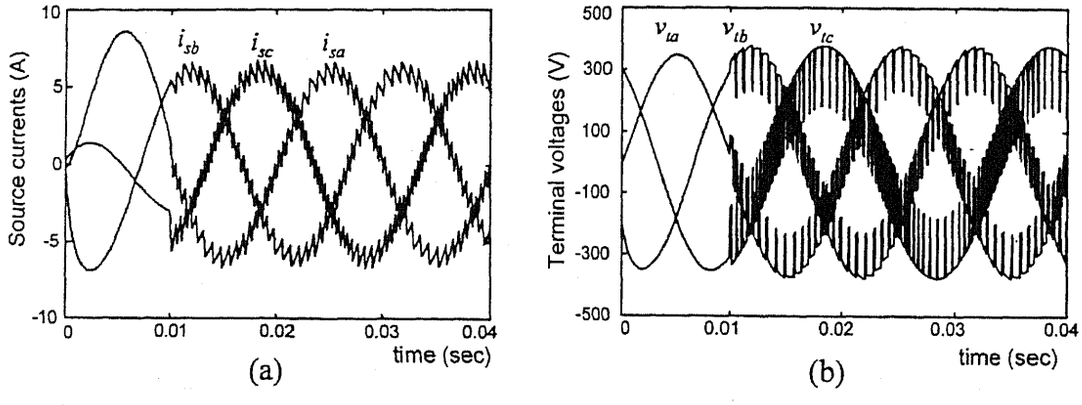


Fig. 5.5 (a) Compensated source currents (b) Terminal voltages after compensation

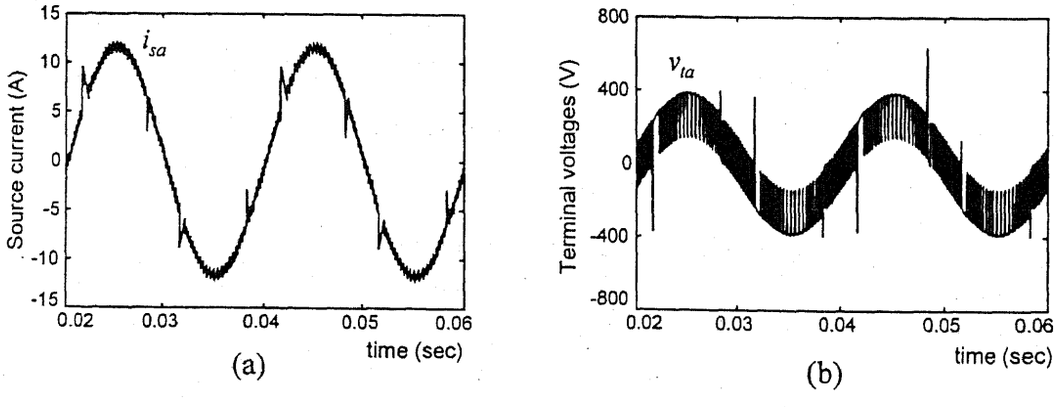


Fig. 5.6 (a) Source current (b) Terminal voltage in phase-a with rectifier load

5.3 USE OF FILTER CAPACITOR TO MINIMIZE THE DISTORTIONS IN TERMINAL VOLTAGES

In the previous section we have seen that, extracting positive sequence of the terminal voltage and feeding it to the shunt algorithm results in better compensated source currents. However terminal voltages still remain contaminated with the inverter switching frequency components. To eliminate these switching frequency components, we must provide a path for them. We therefore use a filter capacitor in each phase that is connected in shunt at the PCC and also use the positive sequence extraction of the terminal voltages. The single phase equivalent circuit is shown in Fig. 5.7 (a) while its Thevenin equivalent is shown in Fig. 5.7 (b).

Thevenin equivalent circuit parameters are as follows.

$$v_s' = \frac{-jX_{cf}}{Z_s - jX_{cf}} v_s \text{ and } Z_s' = \frac{-jZ_s X_{cf}}{Z_s - jX_{cf}} \tag{5.2}$$

where Z_s is the feeder impedance, X_{cf} is the reactance of the filter capacitor. Their values are given as follows.

$$Z_s = R_s + j X_s = R_s + j \omega L_s \text{ and } X_{cf} = 1/\omega C_f$$

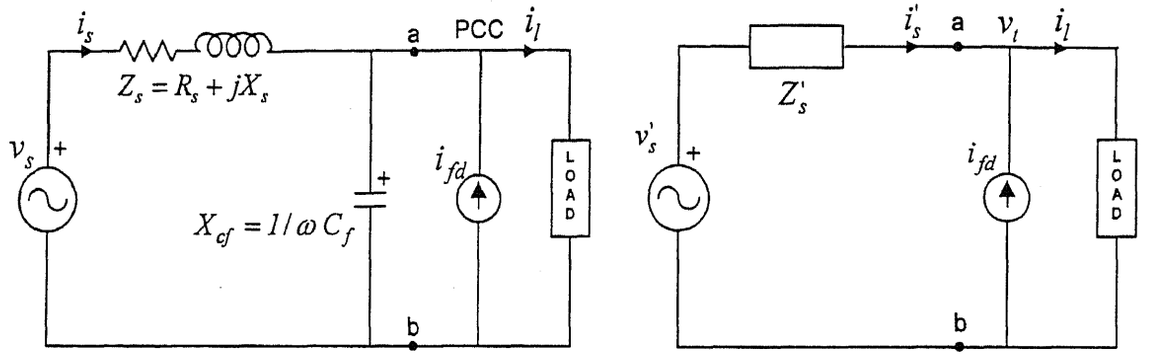
Considering lossless feeder i.e. $R_s = 0$, the Thevenin source voltage and feeder impedance are given as

$$v_s' = -\frac{X_{cf}}{X_s - X_{cf}} v_s \text{ and } Z_s' = \frac{-jX_s X_{cf}}{X_s - X_{cf}} \tag{5.3}$$

It must be ensured that the feeder inductance L_s and the capacitor C_f do not resonate at the fundamental frequency of $f = 50$ Hz ($\omega = 2\pi f$). If the filter capacitor resonates with the feeder reactance at a frequency ω_r, then we get,

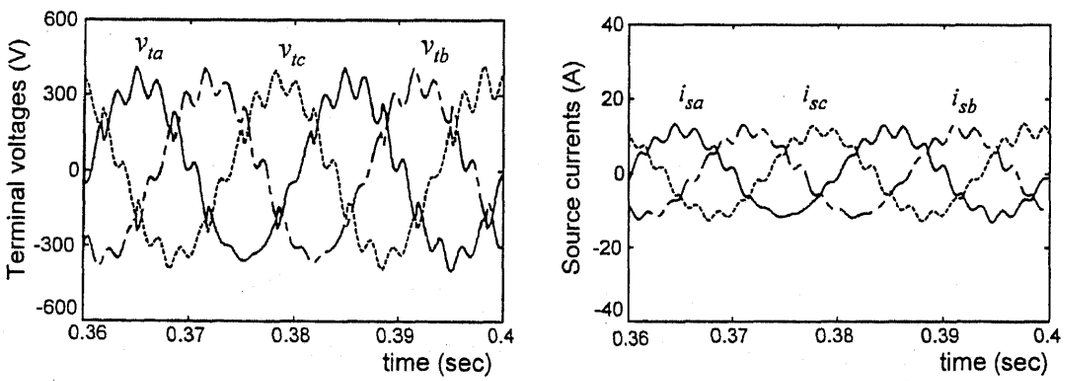
$$C_{fr} = \frac{1}{\omega_r^2 L_s} \tag{5.4}$$

Let us assume that this value is equal to C_{fo} when ω_r is equal to the fundamental frequency (ω_o). The filter capacitor C_f should never be chosen near C_{fo}. This can be achieved by either $C_f << C_{fo}$ or $C_f >> C_{fo}$. However if C_f is very large, the impedance between PCC and ground becomes very small resulting in excessive currents through filter capacitors. Therefore the choice of $C_f >> C_{fo}$ is invalid. We must therefore restrict C_f to be much smaller than C_{fo}. The feeder inductance is $L_s = 0.01$ H for the simulated system. Therefore from (5.4), C_{fo} is 1000 μF for $f_r = f_o = 50$ Hz. Satisfying condition $C_f << C_{fo}$, we can choose C_f to be less than or equal to 200 μF.



(a) (b)

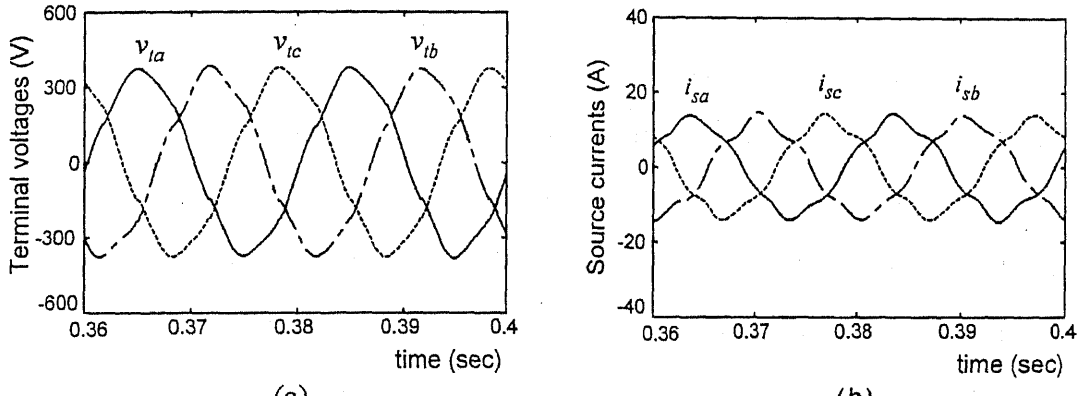
Fig. 5.7 (a) Single line diagram of system with capacitor filter (b) Thevenin circuit looking into terminals a-b



(a) (b)

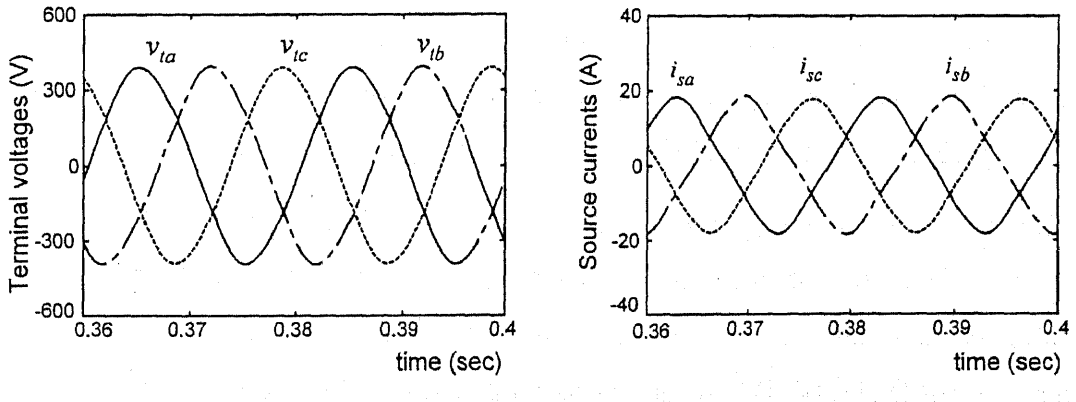
Fig. 5.8 (a) Terminal voltage (b) source current in phase-*a* at C_f= 10 μF

When a small ac capacitor is placed at the point of common coupling, for the same system parameters as given in Table 5.1 (with three-phase diode rectifier drawing output current of 5 A), the switching distortion in terminal voltage as well in source current becomes less. These are shown in Fig. 5.8 (a) and (b) for C_f = 10 μF. The distortion is reduced because the filter capacitor absorbs most of the switching frequency harmonic components and leaves only low frequency harmonic components on the terminal side. Similar waveforms of terminal voltage and source current for some other values of filter capacitor have been obtained. These are shown in Fig. 5.9 to Fig. 5.11 for capacitor values of 50 μF, 100 μF and 200 μF respectively.



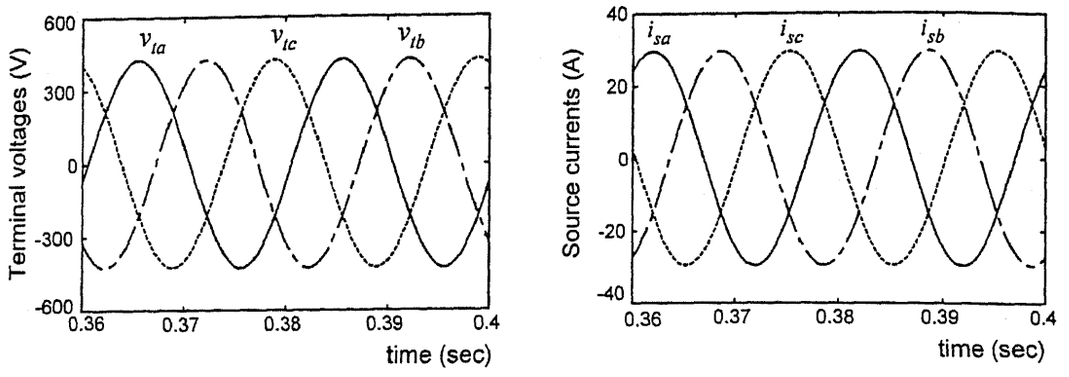
(a) (b)

Fig. 5.9 (a) Terminal voltage (b) Source current in phase-*a* at C_f = 50 μF



(a) (b)

Fig. 5.10 (a) Terminal voltage (b) Source current in phase-*a* at C_f = 100 μF



(a) (b)

Fig. 5.11 (a) Terminal voltage (b) Source current in phase-a at C_f = 200 μF

From these figures it can be seen that as the value of filter capacitor increases, the distortion in the voltage and current decreases. This is obvious since for a particular harmonic frequency the reactance of the capacitor reduces with increase in the value of C_f creating a low impedance path for harmonic current. But at the same time, this increase in the value of C_f implies that reduction in the value of fundamental reactance of the filter capacitor creates a low impedance path for the fundamental current as well. Furthermore, as explained before, an increase in the value of C_f pushes the system towards series resonance. Therefore it will result in increase of both terminal voltage and source current. It can be seen from Fig. 5.11 (a) that the terminal voltage peak reaches about 430 V against peak value of 360 V in the source. The source currents are shown in Fig. 5.11 (b). It is observed from the figure that peak of source current reaches to 30 A, while the load requires a peak currents of 14 A, 12 A and 8 A in phases a, b and c respectively.

It is therefore clear that a straightforward insertion of a fixed capacitor at PCC does not solve our problem. On the other hand, connecting a shunt capacitor at this PCC is the only cost effective solution to provide a path for the switching components. Now let us look at the objective of DSTATCOM operating under a non-stiff source. In this case, assuming the source voltage to be balanced and sinusoidal, a balanced sinusoidal source current implies balanced sinusoidal terminal (PCC) voltage. Therefore, it is desirable to switch the VSI in such a way that both terminal voltage reference and shunt current reference can be tracked simultaneously. This is explained in the next section.

5.4 STATE FEEDBACK CONTROL

In the previous section it was observed that, through positive sequence extraction of the terminal voltages the distortion in the source currents was eliminated. However the terminal voltage still remains distorted. It is therefore imperative to employ the filter ac capacitor to provide a path for the inverter switching frequency current components. Therefore the DSTATCOM circuit given in Fig. 5.1 has been modified as shown in Fig. 5.12.

Let us now consider a compensated system with its single line diagram as shown in Fig. 5.12. There are two shunt branches connected at the PCC–one the DSTATCOM branch and the other consisting of the filter capacitor. The branch currents are denoted by i_{fd} and i_{cf} with their reference direction as indicated in the figure. The difference of these two currents is the shunt current (i_{fl}) injected at the PCC. We must make the current (i_{fl}) to follow the reference current and also force v_{cf} to follow a reference terminal voltage.

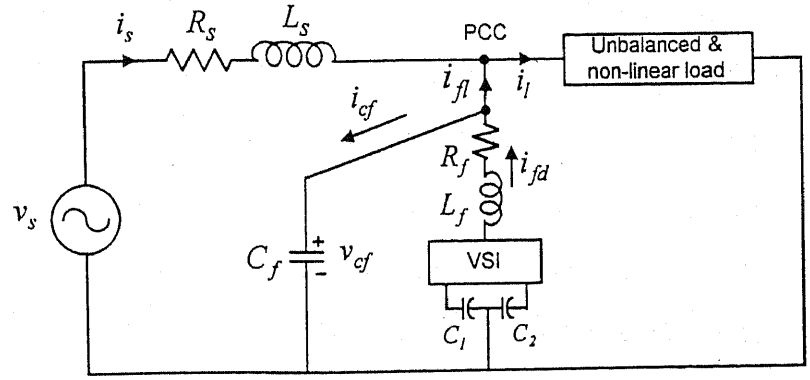


Fig. 5.12 Single line diagram of shunt compensation with filter capacitor

5.4.1 State Space Model

The equivalent circuit of the compensated system shown in Fig. 5.12 is given in Fig. 5.13. This figure includes a passive R-L load. We define three loops with loop currents i_1, i_2 and i_3 as shown in Fig. 5.13. Then a state vector of the state space equation is defined and it is given as,

$$x^t = [i_1 \;\; i_2 \;\; i_3 \;\; v_{cf}] \tag{5.5}$$

In Fig. 5.13, $V_{dc}^{'} = V_{dc}\, u$, where V_{dc} denotes the voltage across each dc capacitor and u is a switching function generated through feedback control. The state space equation for the compensator with ac filter capacitor can be written as,

$$\dot{x} = \begin{bmatrix} -R_s/L_s & 0 & 0 & -1/L_s \\ 0 & -R_f/L_f & 0 & 1/L_f \\ 0 & 0 & -R_l/L_l & 1/L_l \\ 1/C_f & -1/C_f & -1/C_f & 0 \end{bmatrix} x + \begin{bmatrix} 1/L_s \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s + \begin{bmatrix} 0 \\ -V_{dc}/L_f \\ 0 \\ 0 \end{bmatrix} u \quad (5.6)$$

$$\dot{x} = A\, x + B_1 v_s + B_2\, u \quad (5.7)$$

In this context, the term V_{dc} in (5.6) needs some explanation. For the neutral clamped inverter topology shown in Fig. 5.1, there are two split dc storage capacitors. The voltage across each capacitor is maintained nearly V_{dc}, i.e. $v_{c1} \approx V_{dc}$ and $v_{c2} \approx V_{dc}$. Thus, a total voltage of $2V_{dc}$ is maintained in the dc link. In Fig. 5.1, S and $\bar{S}$ are the status of the switches in top and bottom half of an inverter leg respectively. The switch status S=1 and $\bar{S}$ = 0 implies that the top switch of the inverter leg is closed and it connects inverter to $v_{c1} \approx V_{dc}$, while the bottom switch in the same leg is open. Similarly for S = 0 and $\bar{S}$ =1 the bottom switch connects the inverter leg to $-v_{c2} \approx -V_{dc}$ and top switch in the inverter leg is open. Therefore, through the inverter switching arrangements the inverter supplies a voltage $\pm V_{dc}$. These are represented as $V_{dc}\, u$ in (5.6)

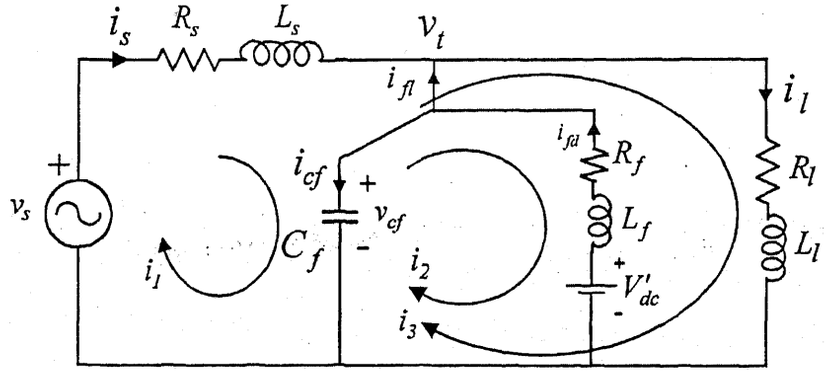


Fig. 5.13 Equivalent circuit of DSTATCOM

The state equation (5.6) contains the feeder impedance, load impedance and compensator parameters. The load impedances are measurable and therefore are known. Due to radial distributed transmission lines, new installations, sudden withdrawal of loads, the feeder impedances are not known and they can change any time. Moreover, any feedback controller must rely mainly on the locally measured variables. For the DSTATCOM shown in Fig. 5.13, the local variables are terminal voltage, source current, filter current, and filter capacitor current. Based on the above observation, we make the use of the following transformation.

$$z = \begin{bmatrix} i_{fl} \\ i_{cf} \\ v_{cf} \\ i_l \end{bmatrix} = \begin{bmatrix} -1 & 0 & 1 & 0 \\ 1 & -1 & -1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} x = \boldsymbol{P}\, x \tag{5.8}$$

The state equation (5.8) can be transformed into

$$\dot{z} = \boldsymbol{PAP}^{-1} z + \boldsymbol{PB}_1 v_s + \boldsymbol{PB}_2 u = \Lambda z + \Gamma_1 v_s + \Gamma_2 u \tag{5.9}$$

Assuming that we have full control over u, an infinite time linear quadratic regulator (LQR) is designed. The control law is defined as,

$$u_c = -\boldsymbol{K}(z - z_{ref}) \tag{5.10}$$

where, z_{ref} is the desired state vector and u_c is the continuous output of the controller. A performance index J is chosen as,

$$J = \int_0^\infty \left\{ (z - z_{ref})' \boldsymbol{Q} (z - z_{ref}) + u_c^t R\, u_c \right\} dt \tag{5.11}$$

The performance index J is minimized to obtain the optimal control law through Riccati equation [79]. For the system parameters considered in Table 5.1 with $L_f = 20$ mH, the following weighting matrices are chosen by trial and error.

$$Q = diag([800 \quad 0 \quad 1 \quad 0]),\ R = 0.06$$

where *diag* is a diagonal matrix. The compensator current i_{fl} and terminal voltages are most important variables in control. The weighting matrix $\boldsymbol{Q}$ reflects the importance of these states. Based on above system and LQR parameters, the gain matrix $\boldsymbol{K}$ is given as $\boldsymbol{K}$ = [106.47 79.59 7.59 −52.49]. Using this state feedback, the oscillatory closed loop eigen values are to the left of the line $\mathrm{Re}(s) = -1298$. To avoid the complexity of forming the reference for the load currents, the gain matrix is restricted to $\boldsymbol{K}$ = [106.47 79.59 7.59]. This reduced state feedback control results in a small shift in the closed loop eigenvalues to the left of the $\mathrm{Re}(s) = -1171$.

5.4.2 Switching Control of VSI of the DSTATCOM

The control signal u_c computed from (5.10) so far using the Linear Quadratic Control (LQR) is a continuous signal. In practice the control signal u is the switching decision of the VSI of the DSTATCOM and thus constrained to be either +1 or −1. This is shown in Fig. 5.14. One important property of the linear quadratic regulator is that it is tolerant of input nonlinearities. The LQR design is stable, provided the effective gain of the input nonlinearity is constrained in the sector between 1/2 and 2 [79]. When the errors are large, and the control is bounded between +1 and −1 the gains of $\boldsymbol{K}$ must be small. The switching control is +1 when the LQR value from (5.10) is positive and −1 when it is negative. For a set of decreasing values of R in (5.11) we get a corresponding set of increasing values of $\boldsymbol{K}$. Thus there will always exist a value of R such that $\boldsymbol{K}\boldsymbol{z}$ is bounded appropriately. Finite time convergence of the regulator problem can be shown, provided $\boldsymbol{Q}$ is chosen such that $R \to 0$, $\boldsymbol{K} \to \infty$. This gives a better performance than the exponential convergence of proportional control.

After the initial transient is over, the control based only on the sign of LQR value will chatter at a rate limited by the switches. To avoid this, the switching is based on,

$$u = hys(u_c) \tag{5.12}$$

where the *hys* function is defined for a small limit (lim) around zero as,

$$\begin{aligned} &if\ w > \lim\ then\ hys(w) = 1 \\ &else\ if\ w < -\lim\ then\ hys(w) = -1 \end{aligned} \tag{5.13}$$

The switching decision of the VSI of the DSTATCOM is thus constrained to be either +1 or −1. It means that either the inverter output is connected to $+V_{dc}$, or $-V_{dc}$. Now, we have to choose the control signal $S = 1$ or 0 and $\bar{S} = 0$ or 1, for value of u corresponding to +1 or −1 respectively, such that the appropriate inverter connection is achieved.

The selection of lim determines the switching frequency while tracking the reference state vector. This gives good convergence to the tracking band as well as good stability of tracking. In this control law the switching decision is based on a linear combination of multiple states. Hence it is named as *switching band tracking control* [23, 80].

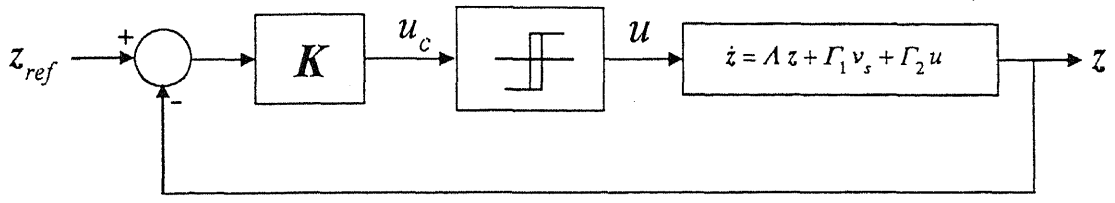


Fig. 5.14 State feedback control with nonlinear element in the forward path

5.4.3 Computation of Reference States

To implement the switching control of (5.10) using the reduced state feedback, we need to compute the reference states, z_{refa}, z_{refb}, z_{refc} for phases *a*, *b* and *c* respectively. The block diagram for reference states computation is shown in Fig. 5.15. The terminal voltages v_{ta}, v_{tb} and v_{tc} are measured and used in positive sequence extraction as described in Section 5.2. The extracted positive sequence voltages are the reference filter capacitor voltages and are denoted as v^*_{cfa}, v^*_{cfb} v^*_{cfc}. From these reference voltages, the reference filter capacitor currents are computed and are denoted as i^*_{cfa}, i^*_{cfb} i^*_{cfc}. The reference compensator currents i^*_{fla}, i^*_{flb} and i^*_{flc} are generated by feeding positive sequence terminal

5.5 SIMULATION RESULTS

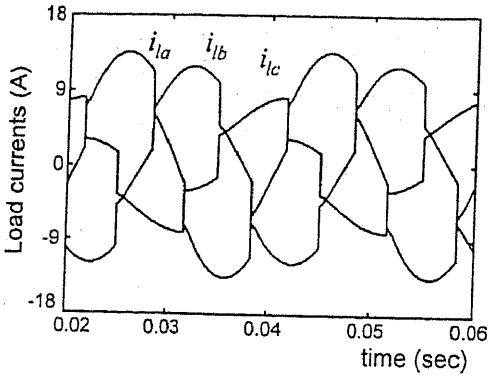
The system parameters for state feedback control of DSATACOM are given in Table 5.2. The voltages of dc capacitors C_1 and C_2 in Fig. 5.12 are assumed to be constant as only steady state results are presented in this section. The load currents for unbalanced R-L and nonlinear load are shown in Fig 5.16 (a). The terminal voltages without any compensation are plotted in Fig. 5.16 (b). The terminal voltages contain the notches due to rectifier load. After compensation based on the state feedback controller the terminal voltages are plotted in Fig. 5.16 (c). The compensated source currents are shown in Fig. 5.16 (d). From Fig. 5.16 (c) and (d) it is inferred that for balanced supply voltages, the terminal voltages and the compensated source currents are balanced and sinusoidal. The reference current and actual currents to be injected through shunt link at PCC are shown in Fig. 5.16 (e). The filter capacitor reference and actual currents are plotted in Fig. 5.16 (f).

Thus it is seen that the state feedback control of DSTATCOM yields better source current and terminal voltage waveforms to those obtained using other methods in non-stiff voltage source conditions.

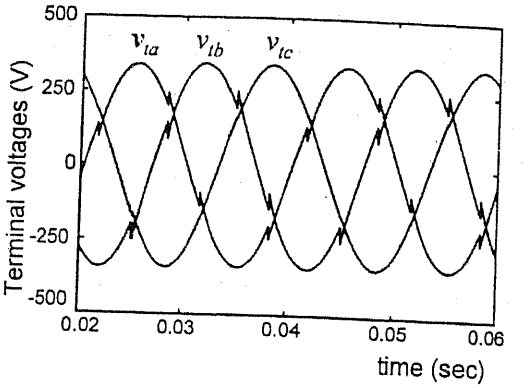
It is mentioned here that state feedback gain matrix $\boldsymbol{K}$ is computed based on phase-*a* parameters. The same gain matrix is used for the phases *b* and *c*.

Table 5.2 System parameters for state feedback control of DSTATCOM

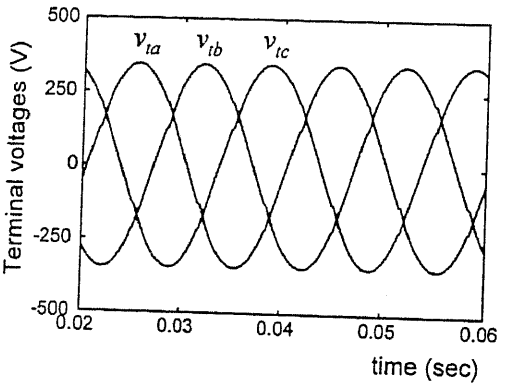
System Parameters	**Values**
System voltage	360 V peak
Load	$Z_a = 40 + j\,5\ \Omega$, $Z_b = 50 + j\,5\ \Omega$, $Z_c = 72 + j\,84\ \Omega$ and a 3-phase diode rectifier drawing current of 5 A
Feeder impedance	$Z_s = 1 + j\,3.14\ \Omega$
DC capacitors	$C_1 = C_2 = 2200\ \mu$F, each capacitor held at 500 V dc
AC filter capacitors	$C_f = 50\ \mu$ F in each phase
Control signal hysteresis band (*lim*)	10



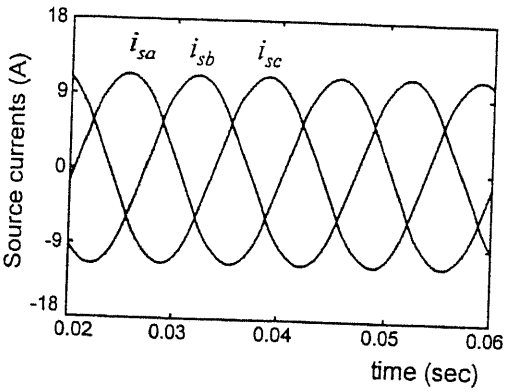
(a)



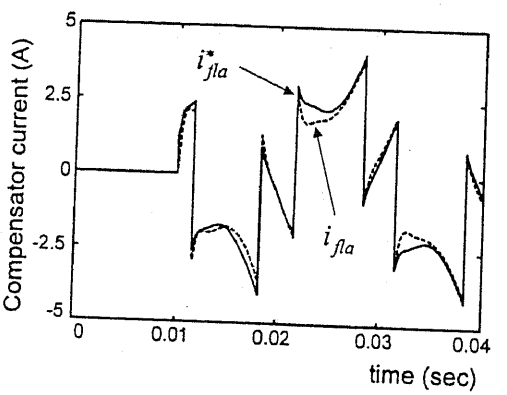
(b)



(c)



(d)



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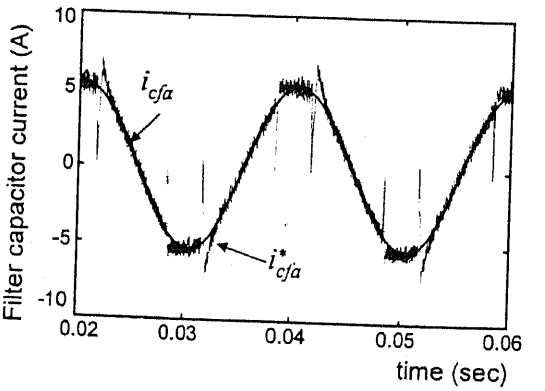


(f)

Fig. 5.16 (a) Load current (b) Terminal voltage before compensation (c) Terminal voltage after compensation (d) Source current after compensation (e) Reference and actual shunt current in phase-*a* (f) Reference and actual ac filter capacitor current in phase-*a*

5.5.1 Additional Robustness Study

The compensator working on state feedback controller is robust as mentioned before. For the load given in Table 5.2, the controller optimal gain for phase-*a* is decided by the LQR. The LQR is designed off-line based on the nominal parameters of the load. To study the robustness of the algorithm the load and the feeder impedance are varied over a wide range. The filter capacitor value is also changed over a wide range. Their effect on the steady state compensator performance has been studied. We discuss three cases below.

Effect of Feeder Impedance on the Compensator Performance

If the feeder impedance reduces, the terminal voltage approaches the source voltage. Since the system becomes stiff, the fundamental extraction is no longer needed. However when the terminal voltages are unbalanced in magnitude and phase angles, a separate algorithm is proposed and verified in Chapter 2 by simulation as well as experimentally.

It was shown in Section 5.1 that for a system with finite feeder impedance, if the shunt algorithm given in Section 2.7 of Chapter 2 is used, it results in terminal voltages and source current contaminated with inverter switching frequency. The use of the state feedback control along with filter capacitor makes the terminal voltage and source current balanced and sinusoidal. The source current can be set to any desired value by substituting proper values of β in (2.75) of Chapter 2. The value of β is set to zero for unity power factor. The source current makes a small angle with source voltage, v_s depending upon the feeder impedance. For large feeder impedance this angle is large. For lower values of the feeder impedance it is small. As the feeder impedance increases, the harmonic contents in terminal voltage and source current also increases. The terminal voltages reduce due to large voltage drop across the feeder impedance.

Two extreme cases of feeder impedance variation are considered. In the first case, the feeder impedance is reduced by a factor of 4 compared to that of feeder impedance given in Table 5.1 (termed as the normal feeder impedance). With this reduced feeder impedance the results are shown in Fig. 5.17 (a)-(b). It is seen from Fig. 5.17 (a) that due to small feeder impedance, the terminal voltage peak is 357 V, which is nearly the peak of system

voltage (360 V). The source currents are however little distorted which implies that for small feeder impedance instead of using state feedback control of DSTATCOM, shunt compensation algorithms as proposed in Chapter 2 can be employed.

In Fig. 5.17 (c)-(d), the results are shown for feeder impedance increased 4 times to its normal value. It can be seen from Fig. 5.17 (c) that the peak of terminal voltage is about 297 V, which is considerably less than the peak of system voltage (360 V). This is due to the large voltage drop across the feeder impedance. The source currents as shown in Fig. 5.17 (d) are balanced and sinusoidal. Thus we see that for a wide range of feeder impedance variation, the DSTATCOM is able to maintain the terminal voltages and source currents balanced and sinusoidal to a large extent.

Effect of Load Impedance Variation on the Compensator Performance

Like PWM inverter control, the state feedback controller also adds switching frequency components. However the switchings of inverter are not directly seen in the terminal and voltage waveforms due to its nature of control. The gain matrix $\boldsymbol{K}$ is same as taken for normal load and feeder impedance as in Sub-section 5.4.1. At very low load currents, compensated source currents are also proportionally low. The load currents are now reduced by a factor of 4 to the normal load currents shown in Fig. 5.16 (a). The terminal voltages and source currents are shown in Fig. 5.18 (a) and (b) respectively. It is observed from these voltage and current waveforms that they are balanced and sinusoidal. Next, the load currents are increased to 200% of normal current. The terminal voltages and source currents are shown in Fig. 5.18 (c) and (d). Due to large load currents, the source currents are also large. However, for large current $L_s \frac{di_s}{dt}$ is also large and a small distortion in the source current amplifies to a large distortion in the terminal voltage. This is evident from Fig. 5.18 (c). However, by and large the distortion in both source current and terminal voltage is within acceptable limit.

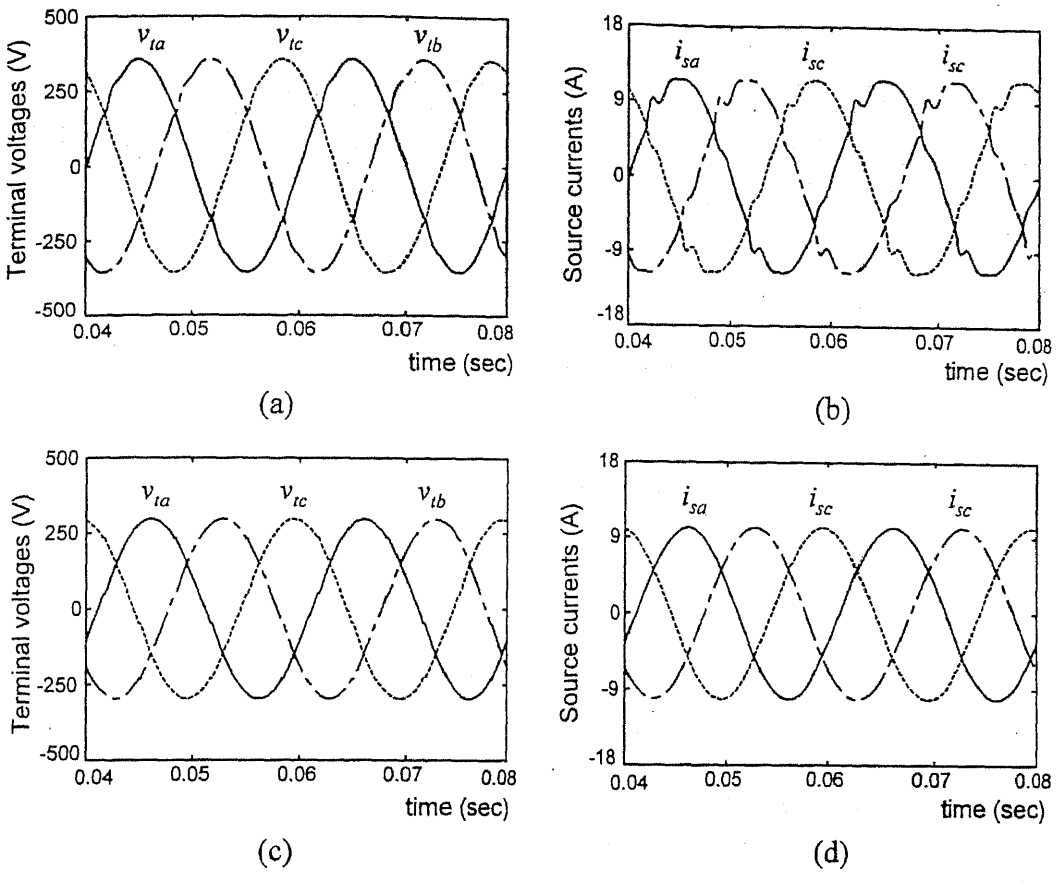


Fig. 5.17 (a) Terminal voltage (b) Source current with feeder impedance reduced by a factor of 4 (c) Terminal voltage (d) Source current at feeder impedance increased by a factor of 4

Effect of Filter Capacitor on the Compensator Performance

The small filter capacitor has less smoothening effect on the terminal voltages and also on the source currents. In this discussion, we consider the same system parameters and the same gain matrix $\boldsymbol{K}$ as computed before for C_f = 50 μF. The terminal voltages and source currents are shown in Fig. 5.19 (a) and (b) respectively when C_f is reduced to 10 μF. It can be seen that the load rectifier switching frequency components appear in both the terminal voltage and source current. However the inverter switching frequency components are (almost) absent from these quantities. If the capacitor value is increased to 200 μF, the terminal voltages and source currents are more smoothened and balanced sinusoids. These are shown in Fig. 5.19 (c) and (d). However, higher filter capacitor has disadvantage that

the inverter currents (i_{fd}) and filter capacitor current (i_{cf}), increase considerably. This means that the inverter and filter capacitor current rating are increased.

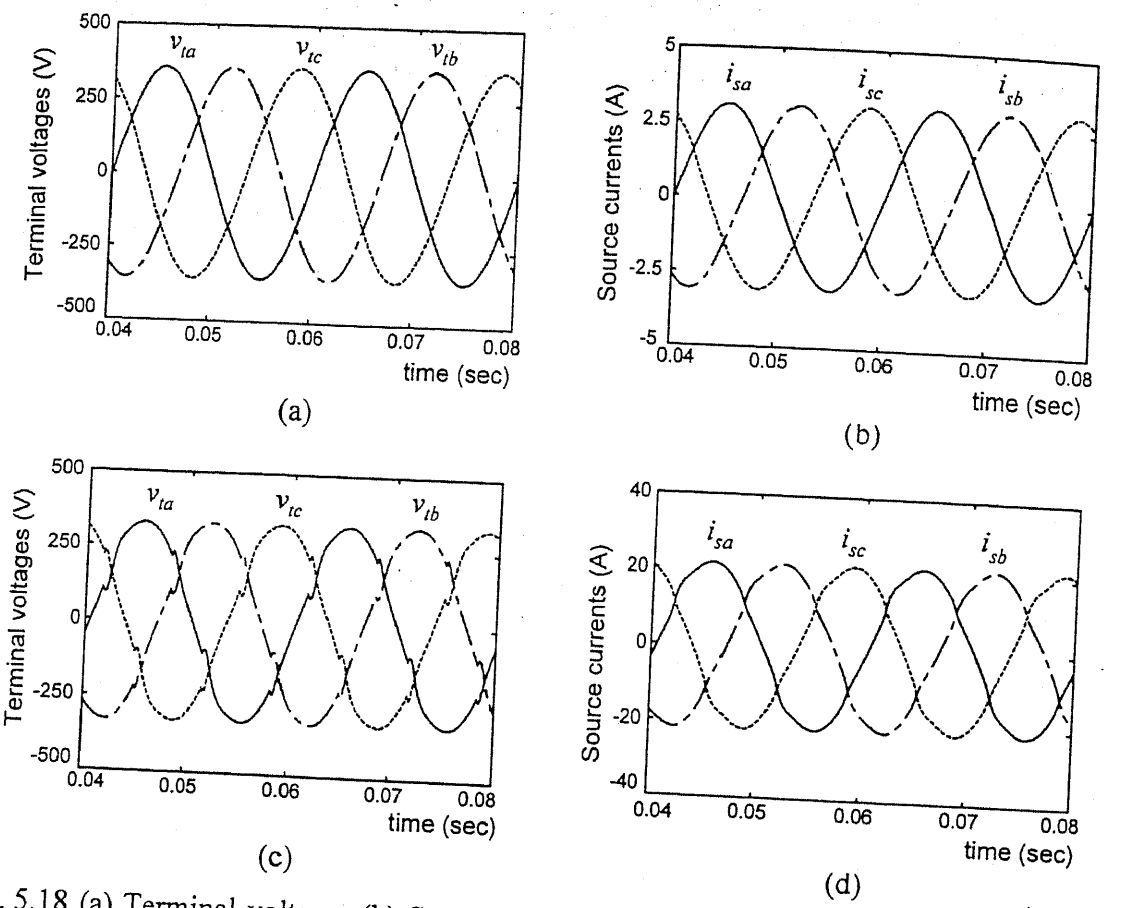


Fig. 5.18 (a) Terminal voltages (b) Source currents with load currents reduced by a factor of 4 (c) Terminal voltages (d) Source currents with load currents increased to double of normal load currents

5.5.2 Performance of Compensator under Unbalanced Source Voltages

The algorithm used here assumes that the source voltages are balanced and so are the feeder impedances. The uncompensated terminal voltages may be unbalanced and may contain harmonics depending upon the feeder impedance and load impedance and harmonic in the load currents. However as shown, PCC voltage can be made balanced if the compensator works perfectly provided the source voltage and feeder impedance are balanced. But if there is unbalance and harmonic in the source voltages, it will result in unbalance in source currents as well as in the terminal voltages. The performance of the compensator with balanced supply sources has been discussed in previous section. In the subsequent

discussion, the effects of unbalanced feeder and unbalanced and distorted source voltage on the compensator performance are studied.

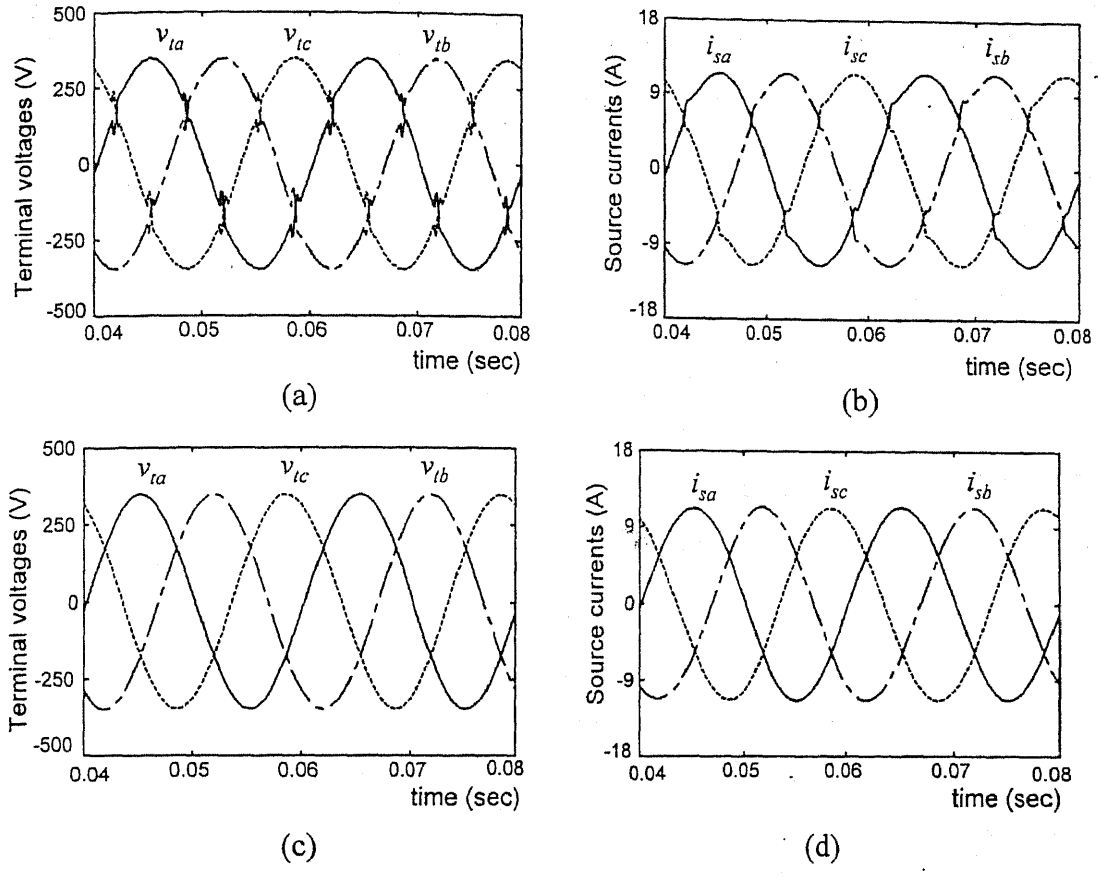


Fig. 5.19 (a) Terminal voltages (b) Source currents at $C_f = 10$ μF instead 50 μF (c) Terminal voltages and (d) Source currents at $C_f = 200$ μF instead 50 μF

Unbalance in Feeder Impedance

As has been pointed out that for balanced source voltage and balanced feeder impedance, the DSTATCOM operation gives balanced and sinusoidal terminal voltages and source currents. If the feeder impedances in three phases are not balanced, the terminal voltages and source currents are also affected. The normal value of feeder impedance is given in Table 5.1. Now, the feeder impedance in phase-*b* is increased to twice, while the feeder impedance in phase-*c* is reduced by a factor of 2 from its normal value. Feeder impedance in phase-*a* remains same. For these feeder impedances, the compensated terminal voltage and source currents are shown in Fig. 5.20 (a) and (b) respectively. It is observed in these

figures that due to unbalance in feeder impedance, the terminal voltages and source currents are unbalanced.

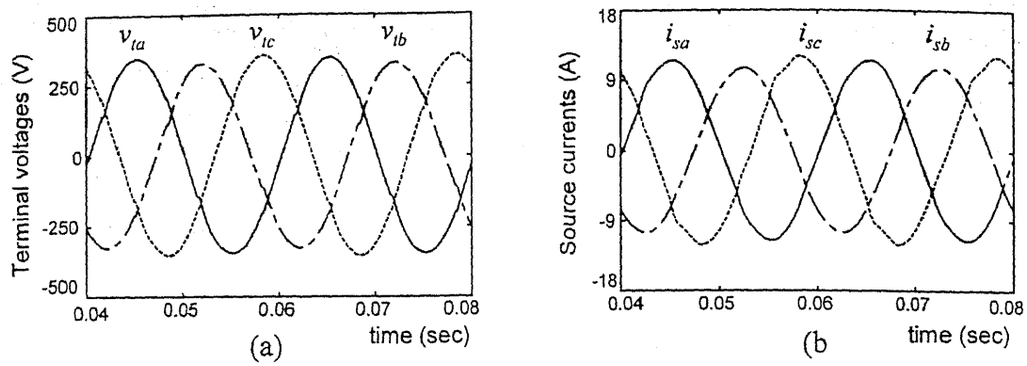


Fig. 5.20 (a) Terminal voltages (b) Source currents for unbalance feeder

Source Voltage Containing Harmonics

The source voltage contains 4% third harmonic in each phase i.e. the source voltages are given by

$$v_{sa} = 360\{\sin(\omega t) + 0.04\sin(3\omega t)\}$$
$$v_{sb} = 360\{\sin(\omega t - 120°) + 0.04\sin(3(\omega t - 120°))\}$$
$$v_{sc} = 360\{\sin(\omega t + 120°) + 0.04\sin(3(\omega t + 120°))\}$$

The load consists of R-L unbalanced load as given in Table 5.1. Now we run the same state feedback control algorithm for the above load and system voltage. The simulated results are plotted in the following figures. The source voltages are shown in Fig. 5.21 (a). The terminal voltages are shown in Fig. 5.21 (b). The compensated source currents are shown in Fig. 5.21 (c) and Fig. 5.22 (a) and (b). It is seen from Fig. 5.21 (c) that, the source currents appear to be flat top and distorted. This is because the third harmonic in the source currents is relatively large as compared to fundamental. If the load is increased the distortion disappears as seen in Fig. 5.22 (a) where R-L load has been reduced to $1/4^{th}$ of the values given in Table 5.1.

Another way to remove this distortion from the source currents is to generate the source voltage harmonics in the PCC voltages. It requires the measurement of harmonics in the source voltages and adding these harmonics to the reference filter capacitor voltages and currents. However this makes the system operation more complex. The simulated source currents for this case are shown in Fig. 5.22 (b), where 4% third harmonic has been added

to the reference for terminal voltages and capacitor currents in the vector z_{ref}. However, for the generation of reference compensator currents only positive sequence terminal voltages have been used.

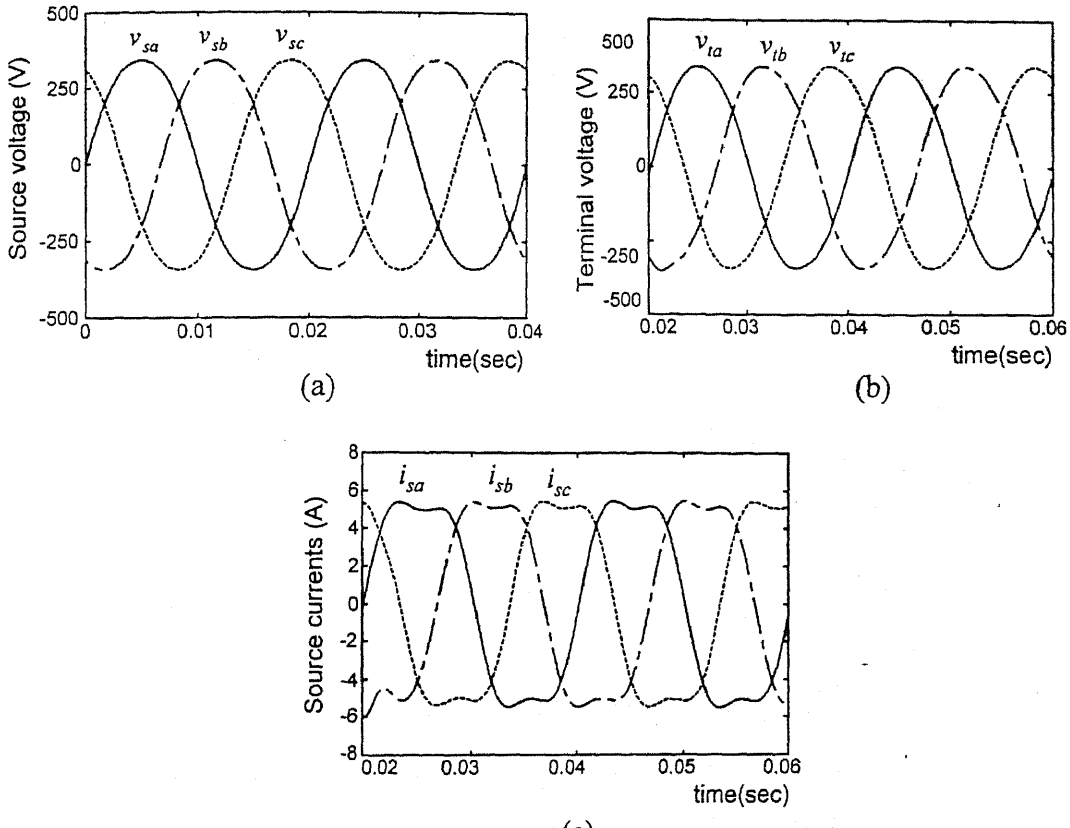


Fig. 5.21 (a) Source voltages with 4% third harmonic (b) Terminal voltages (c) Source currents after compensation

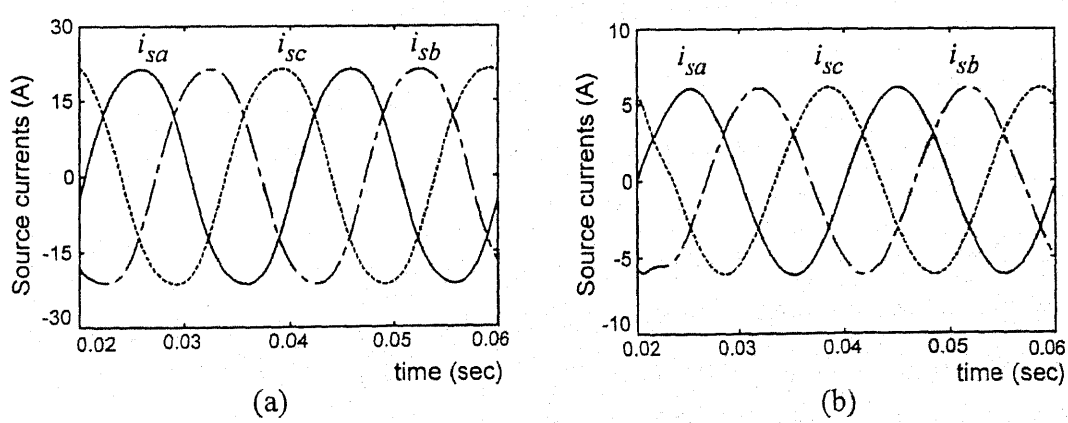


Fig. 5.22 Source currents with (a) Increased load currents (b) Unchanged load currents and harmonics in PCC voltages

Now in addition to R-L load, three-phase full bridge diode rectifier load drawing 5 A current is also considered. For this load the terminal voltages and the source currents are shown in Fig. 5.23 (a) and (b) respectively. As discussed earlier, due to significant third harmonic component in the source currents, their waveforms are flat top and distorted. However, the source currents can be made sinusoidal and balanced if source voltage harmonics are generated in PCC voltage.

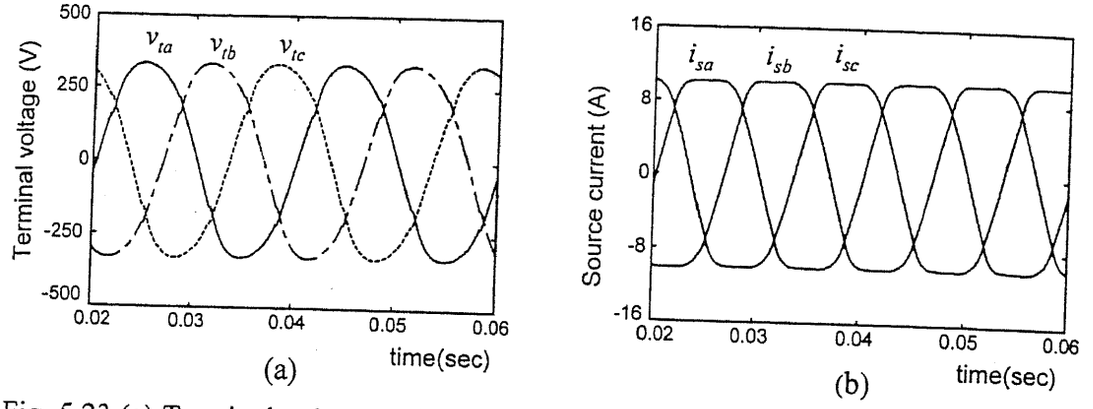


Fig. 5.23 (a) Terminal voltages with additional diode rectifier load (b) Source currents

Source Voltage Containing Unbalance and Harmonics

In this section, in addition to the 4% third harmonic component, the magnitude unbalance in source voltages is also considered. The source voltage equations are:

$$v_{sa} = 360\{\sin(\omega t) + 0.04\sin(3\omega t)\}$$
$$v_{sb} = 345\{\sin(\omega t - 120°) + 0.04\sin(3(\omega t - 120°))\}$$
$$v_{sc} = 374\{\sin(\omega t + 120°) + 0.04\sin(3(\omega t + 120°))\}$$

The unbalance source voltages are plotted in Fig. 5.24 (a). The load parameters are same as given in Table 5.2. The load currents shown in Fig. 5.16 (a) will accordingly change. The terminal voltages before and after the compensation are shown in Fig. 5.24 (b) and (c) respectively. The source currents after compensation are shown in Fig. 5.24 (d). The distortion in source currents can be explained similarly as in the previous discussion in reference to Fig. 5.21 (c). However, it is observed from Fig. 5.24 (d) that the source currents are less distorted compared to the load currents shown in Fig. 5.16 (a).

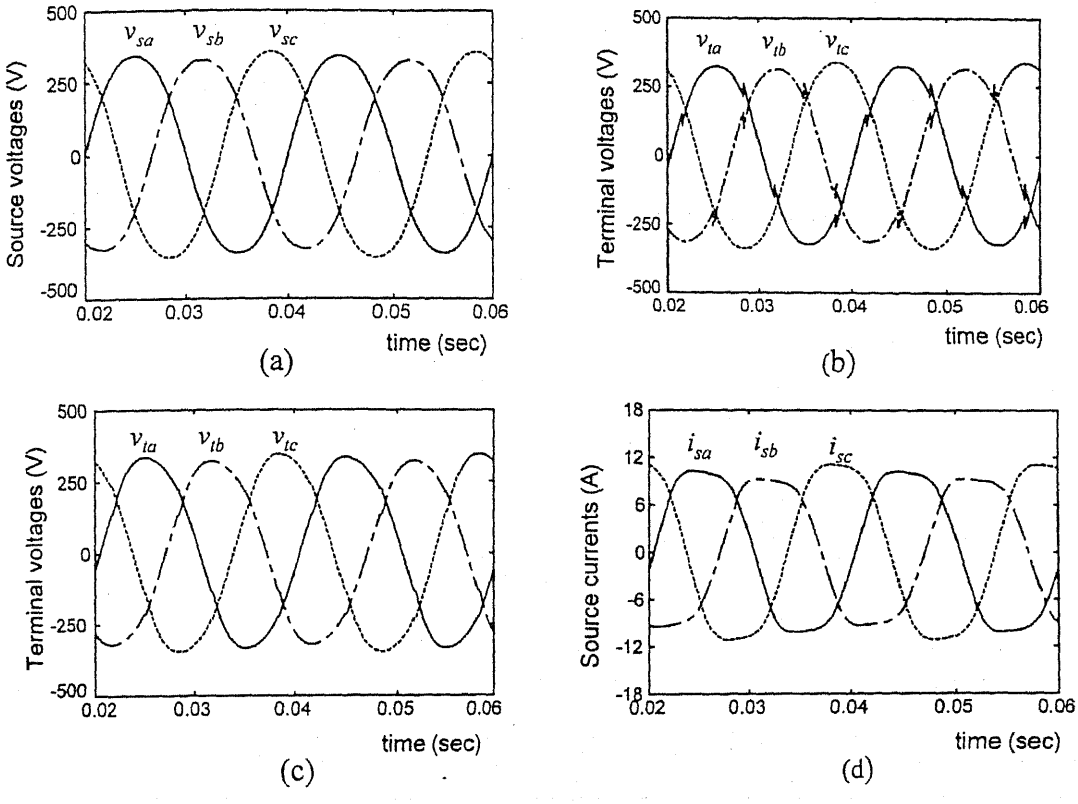


Fig. 5.24 (a) Source voltages (b) Terminal voltages before compensation (c) Terminal voltages after compensation (d) Source currents after compensation

5.6 EXPERIMENTAL RESULTS

The experiments are performed at voltage reduced by a factor of 10 and compared with full scale simulation. Thus the source voltages are nearly sinusoidal with a peak of 36 volts. This is adjusted using three-phase dimmerstat. The load parameters are shown in the Table 5.3. The quality of commercial supply obtained from the mains is such that, the three-phase source voltages are not perfectly balanced and sinusoidal. The source voltage waveforms are given in Fig. 5.25. It can be seen that they are not exactly balanced. In addition, they also contain 3rd harmonic. The system voltages v_{sa}, v_{sb}, v_{sc} and load current i_{la}, i_{lb}, i_{lc} are sensed using Hall effect voltage and current transducers. The voltage and current signals are acquired by PC (P-II, 350 MHz) through data acquisition card (9118 DG

NuDAQ). The algorithm for reference filter currents is implemented in Turbo C/C++. To obtain the average load power ($\bar{p}_l$), moving average filter has been used. To obtain the positive sequence components, ($v_{tal}, v_{tbl}, v_{tcl}$), from the terminal voltages (v_{ta}, v_{tb}, v_{tc}) the procedure given in Section 5.2 is adopted. Then, filter reference currents are generated using algorithm given in Section 2.7 of Chapter 2.

Table 5.3 System parameters of the experimental system

Experimental system Parameters	Values
System voltages	36 V peak
Load	$Z_a = 40 + j\ 0\ \Omega$, $Z_b = 50 + j\ 0\ \Omega$, $Z_c = 72 + j\ 84\ \Omega$ and a 3-phase diode rectifier drawing current of 0.5 A
Feeder impedance	$R_s = 1\ \Omega$, $L_s = 10$ mH
Interface impedance	$R_f = 1\ \Omega$, $L_f = 40$ mH and 20 mH
DC capacitors	2200 μF each
Current hysteresis band	0.04 A
AC filter capacitors	50 μF in each phase
Control signal hysteresis band (lim)	1

The steady state uncompensated load currents are shown in Fig. 5.26. As seen from this figure, the load currents are unbalanced and contain harmonics due to unequal load impedances given in Table 5.3. The uncompensated terminal voltages are shown in Fig. 5.27. It is observed from this figure that the terminal voltages contain notches due to rectifier load. The small unbalance in these voltages is due to the unbalance in source voltages, and unbalanced load. In addition, three separate R-L impedances have been used for simulating the feeder. Even though their values are chosen to be equal, it can not be guaranteed that they are identical. Thus, without any compensation, the non-stiff source produces source currents (which are also the load currents), that are unbalanced and contain harmonics. Similarly, the terminal voltages are also unbalanced and contain harmonics.

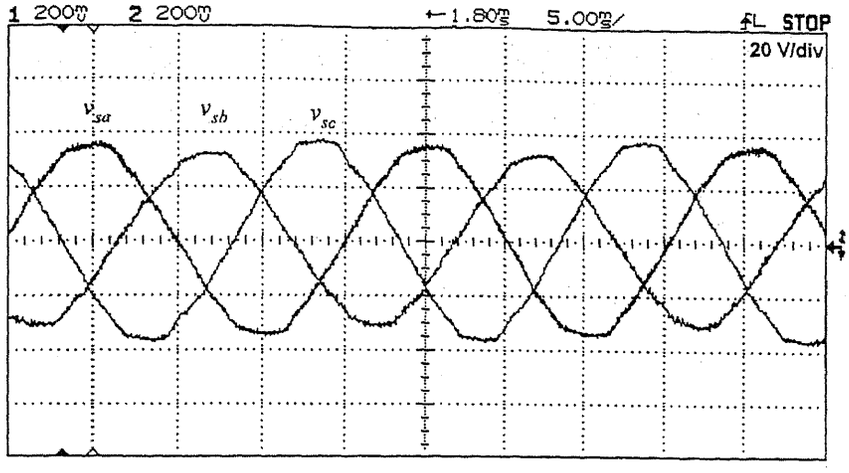


Fig. 5.25 Source voltages of the system

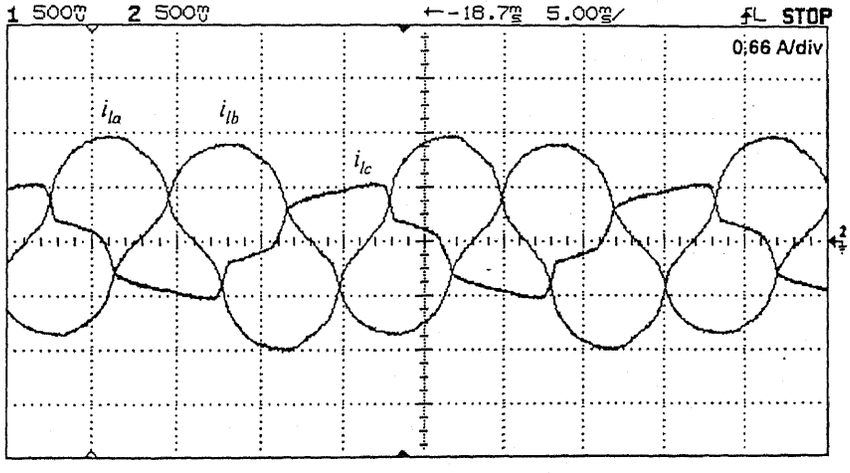


Fig. 5.26 Three-phase load currents

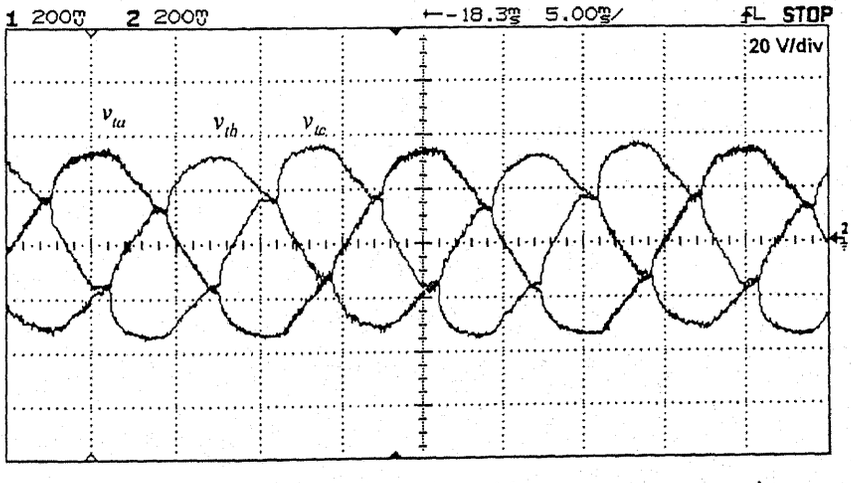


Fig. 5.27 Terminal voltages without any compensation

5.6.1 Performance of the Compensator with Shunt Algorithm

When we employ the shunt algorithm given in Section 2.7 directly without any filter capacitor or state feedback control or fundamental extraction, the terminal voltage and source current in phase-a are shown in Fig. 5.28. We see in this figure that the terminal voltages and the source current are both distorted. Similar is the case for phases b and c. The terminal voltages contain the switching frequency components and so does the source currents. Also the pattern of switching of the inverter is very irregular. It can be seen that this experimental result is similar to the simulation result shown in Fig. 5.2 (b) and (c).

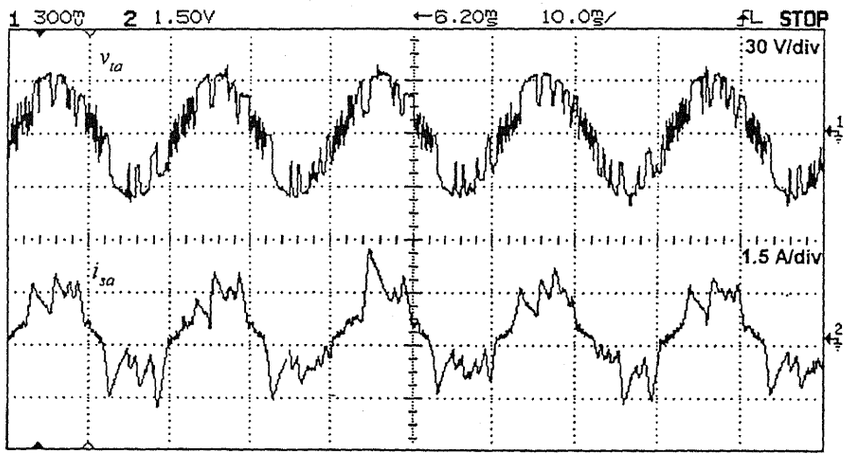


Fig. 5.28 Terminal voltage and source current in phase-a with direct application of shunt algorithm

5.6.2 Performance of the Compensator with Shunt Algorithm and Fundamental Extraction

We now extract the positive sequence components ($v_{ta1}, v_{tb1}, v_{tc1}$) of the terminal voltages using the procedure given in the Section 5.2 and use it in the shunt algorithm of Section 2.7. We still do not employ a filter capacitor or state feedback control. The voltage and source current waveforms in phase-a after compensation are shown in Fig. 5.29. It is observed from this figure that with positive sequence extraction of the terminal voltages and using these improved signals in the shunt algorithm, the source current becomes nearly sinusoidal, albeit containing inverter switching frequency. It has a regular pattern of

switching and a cleaner waveform as compared to the waveform in Fig. 5.28. The source currents in phases *a*, *b* and *c* are shown in Fig. 5.30. However, the terminal voltage still remains distorted due to presence of inverter switching frequency components and the finite feeder impedance.

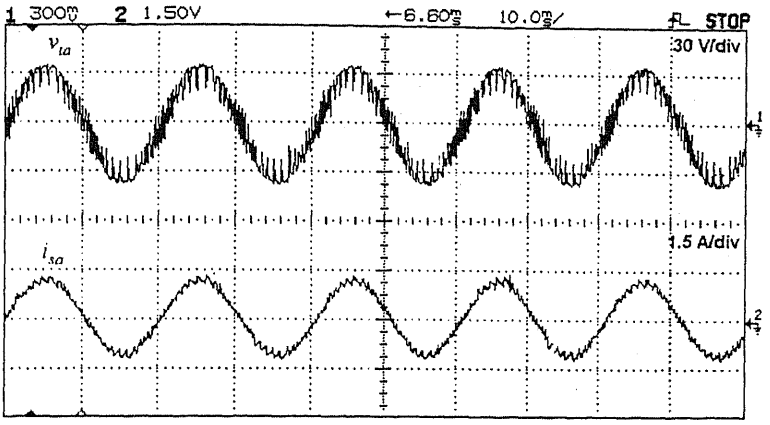


Fig. 5.29 Terminal voltage and source current with positive sequence extraction

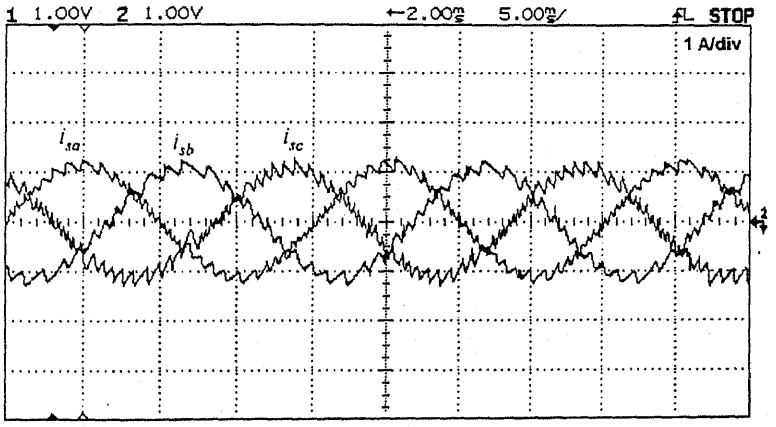


Fig. 5.30 Three-phase compensated source currents with positive sequence extraction

We now intentionally create an unbalance in the supply voltages. This is created by employing two single phase variacs in addition to three-phase variac. The amplitudes of source voltages are unbalanced by 10%. The unbalanced supply voltages are shown in Fig. 5.31. The three voltages are not perfectly sinusoidal and also contain harmonics. The positive sequence components are extracted from unbalanced terminal voltages to implement the shunt algorithm. The terminal voltages and the source currents are shown in Figs. 5.32 and 5.33 respectively. We see here that for this 10% unbalance in the source voltages, the shunt algorithm gives good result as far as source currents are concerned.

However, the unbalance of the source voltages is also passed on to the terminal voltages in addition to distortion due to switching of the inverter and finite feeder impedance as seen in Fig. 5.32. The peak terminal voltage in phase-*a* is 34 V, while as that of phases-*b* and *c* are 30 V and 37.5 V respectively.

The results shown in Figs. 5.32 and 5.33 are similar to those shown in Fig. 5.6 (b) and (a) respectively. In Fig. 5.6 (a) and (b) there are sharp notches in the waveforms of terminal and current waveforms due to ideal rectifier switchings. These are not clearly seen in experimental results in Figs. 5.31 and 5.32 because of gradual rise in rectifier current during commutation of diodes.

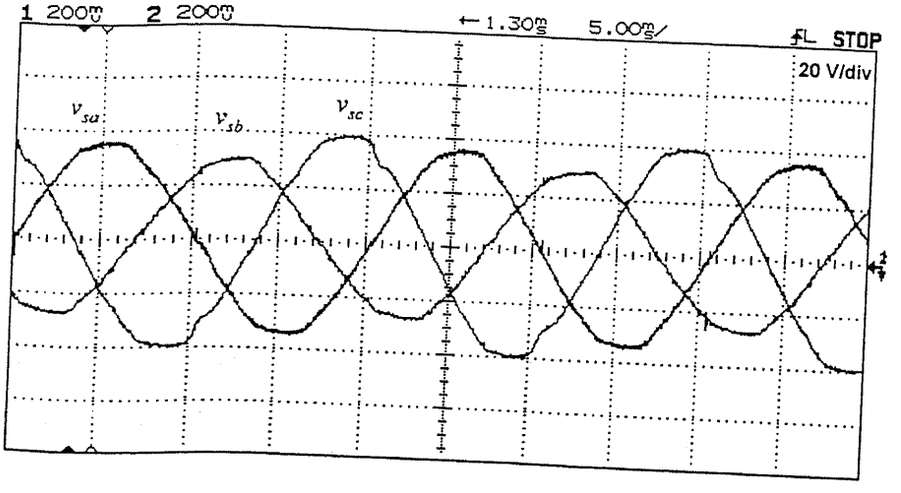


Fig. 5.31 Unbalanced source voltages

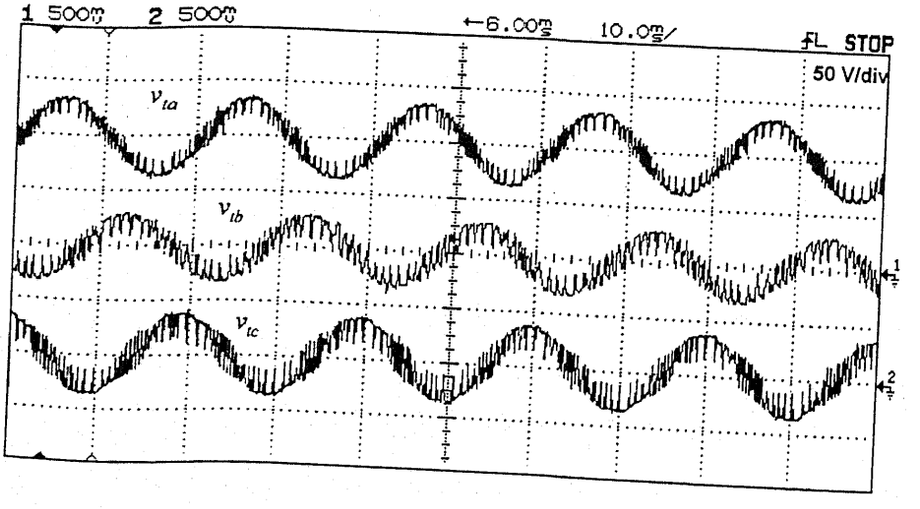


Fig. 5.32 Terminal voltages

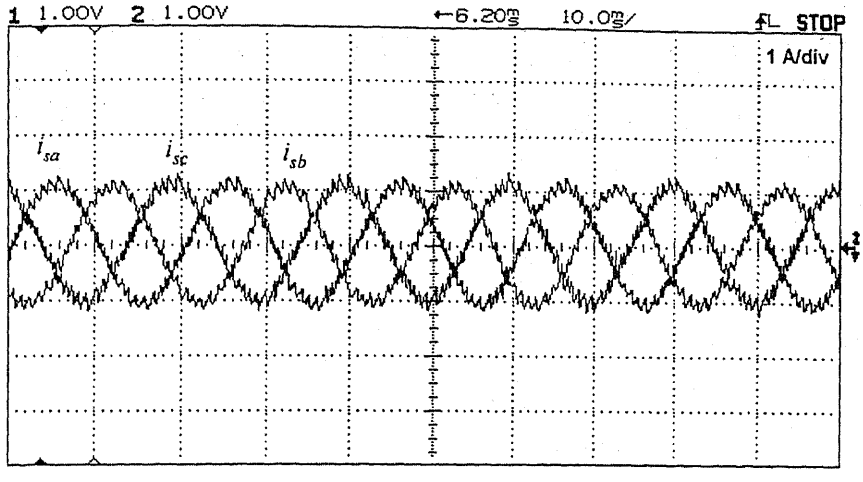


Fig. 5.33 Compensated source currents under more unbalanced voltages

5.6.3 Performance of the Compensator with Shunt Algorithm and Fundamental Extraction with Capacitor Filter at PCC

We now connect a filter capacitor at the point of common coupling (PCC). This is done to remove the distortion in the terminal voltages. The design procedure of filter capacitor and its analysis was carried out in detail in Section 5.3. The performance of the compensator is studied for various values of the capacitor. Here we shall present the experimental results and also compare them with the simulation results.

First we choose value of capacitor C_f equal to 2.5 μF. Terminal and current source waveforms are shown in Fig. 5.34. It is seen from this figure that the switching frequency components are reduced as compared to those without filter capacitor (Fig. 5.29). It is mentioned that in the experiment feeder inductance is chosen as L_s = 0.01 H. For this value and at 50 Hz system frequency the value of the filter capacitor at the resonance (C_{fo}) is 1000 μF. For proper operation with filter capacitor, C_f should be much less than C_{fo} to avoid resonance. It is seen in Fig. 5.34 that the small ac filter capacitor reduces the switching frequency component in terminal voltage and source currents. This has been discussed in detail in Section 5.3. For C_f = 5 μF, the terminal and current waveforms are shown in Fig. 5.35.

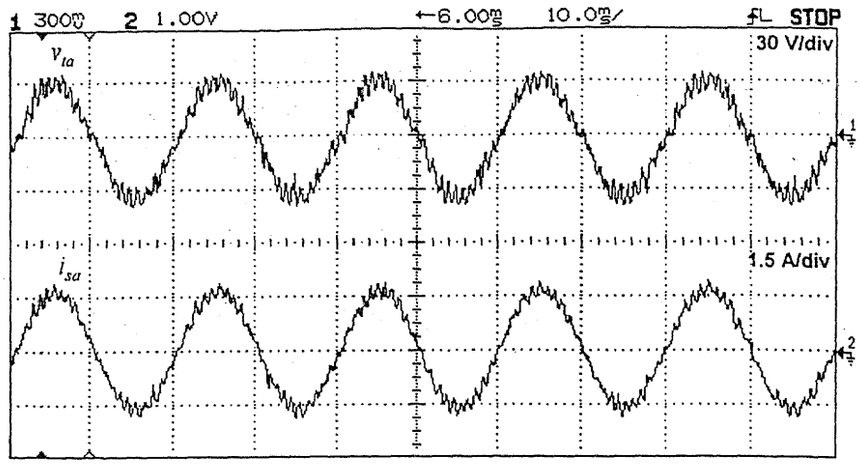


Fig. 5.34 Terminal voltage and source current in phase-*a* for C_f = 2.5 μF

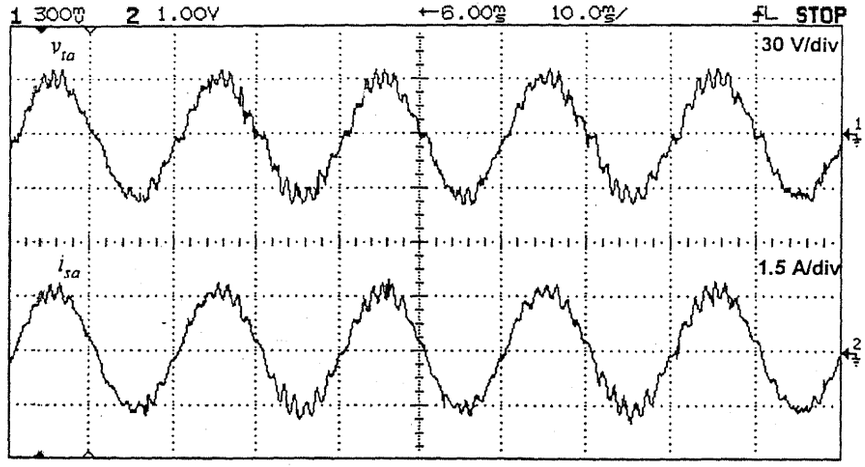


Fig. 5.35 Terminal voltage and source current in phase-*a* for C_f = 5 μF

Similarly the experiments have been carried for values of C_f = 16.0, 24.0 μF. The terminal voltage and current waveforms of phase-*a* are plotted in Fig. 5.36 and 5.37 respectively. From these results it is inferred that as filter capacitor value is increased the switching frequency components in terminal voltage as well as in source current become less dominant. These results are similar to those given in Section 5.3.

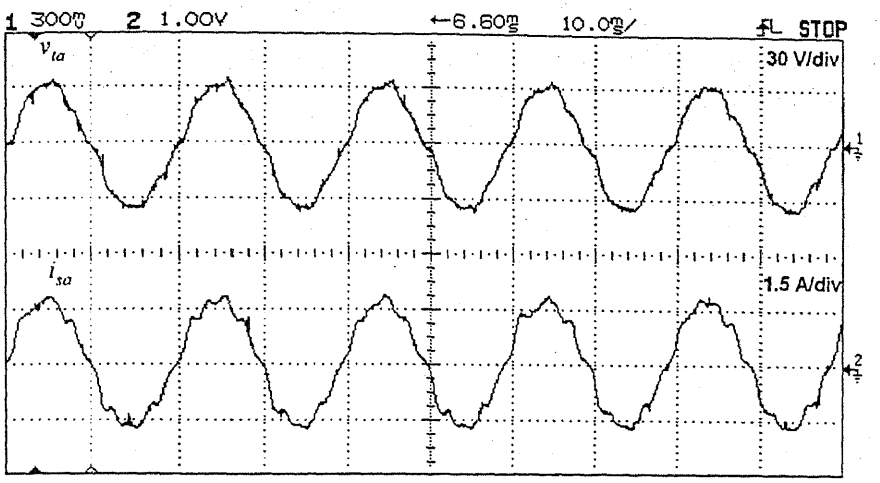


Fig. 5.36 Terminal voltage and source current in phase-*a* for $C_f = 16$ μF

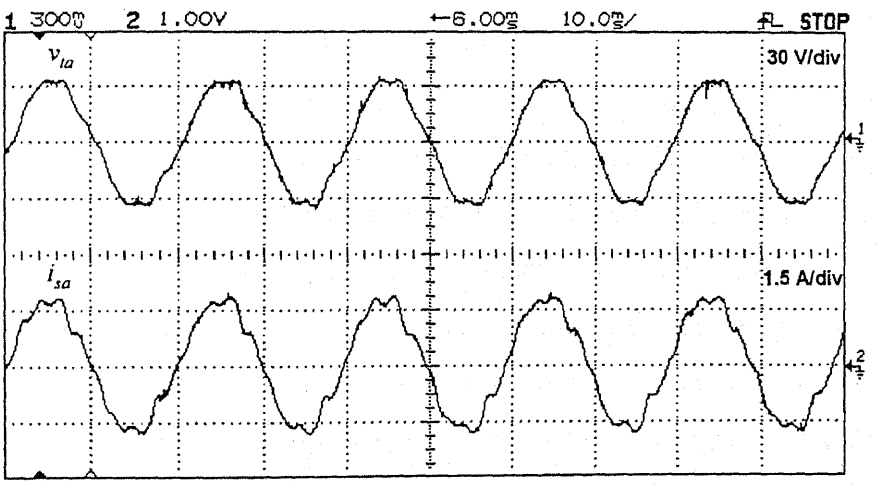


Fig. 5.37 Terminal voltage and source current in phase-*a* for $C_f = 24$ μF

5.6.4 Performance of the Compensator with the State Feedback Control of DSTATCOM

In this section we shall present the experiment results for operating DSTATCOM using state feedback control that is described in detail in Section 5.4. The detailed simulation results have been presented in Section 5.5. From this detailed analysis it is concluded that this is the ideal scheme for load compensation under balanced 'upstream' source voltages.

When the source voltages are unbalanced, those unbalances are passed on the terminal voltages and hence to the source currents as well. Nevertheless the terminal voltage and current waveforms are still free from the inverter switching frequency components. If the unbalance and distortion in source voltages are not severe, the state feedback control algorithm maintains sinusoidal voltages at the terminal bus. But the source current, which can be computed by subtracting terminal voltage from the source voltage divided by feeder impedance, contains the small unbalance and harmonics of the source voltage. It is obvious, as the customer cannot pay for what source is supplying, the price is to be paid by the utility is in terms of quality of source currents. In the following experimental results, the source voltages are same as given in Fig. 5.25. The load configuration and other parameters are same as given in Table 5.3.

Since the system parameters given in Table 5.3, for the experiments are same as simulation system parameters, the LQR parameters are: $\boldsymbol{Q} = [800 \quad 0 \quad 0 \quad 1]$ and $R = 0.06$ as described in Sub-section 5.4.1. The reduced feedback gain matrix $\boldsymbol{K}$ is [106.47 79.59 7.59]. With this state feedback controller, terminal voltages and the source currents for phases *a*, *b* and *c* are plotted in Figs. 5.38, 5.39 and 5.40 respectively. In these figures the load current waveform of the respective phases has also been shown to compare the shapes of these two currents. The three-phase terminal voltages and compensated source currents are separately shown in Figs. 5.41 and 5.42 respectively. It can be observed from Fig. 5.41 that the terminal voltages are nearly balanced and sinusoidal. The source currents as shown in Fig. 5.42, are also nearly balanced and sinusoidal. These contain harmonics due to the small unbalance and distortion in the available source voltage waveforms as shown in Fig. 5.25. It can be seen that the terminal voltages are much better than that of the source voltages of Fig. 5.25. However the source currents are as best as can be achieved in this set-up.

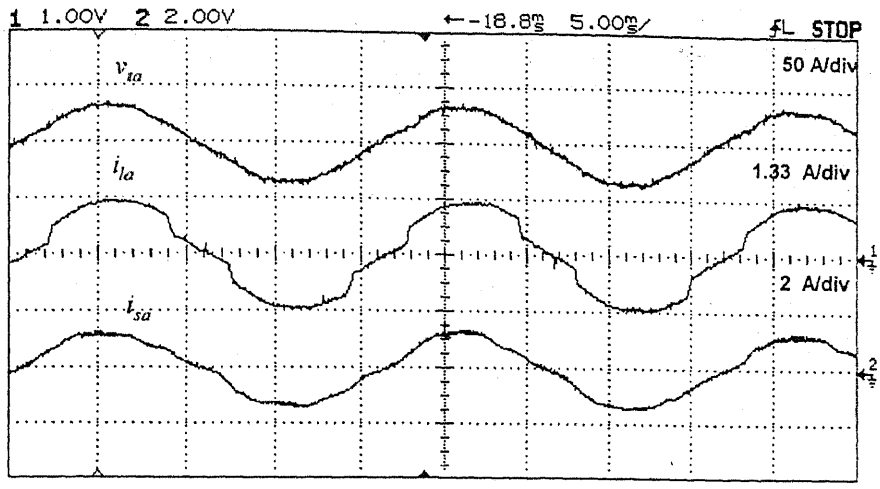


Fig. 5.38 Terminal voltage and source current in phase-*a* with state feedback controller

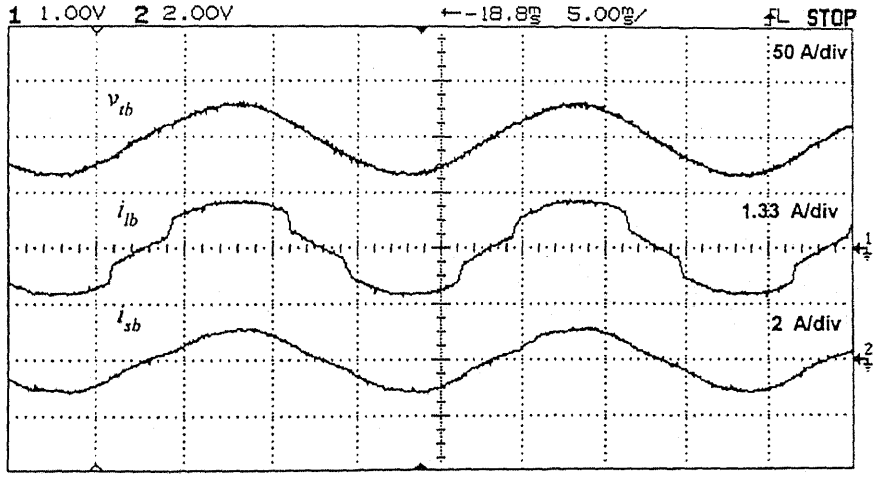


Fig. 5.39 Terminal voltage and source current in phase-*b* with state feedback controller

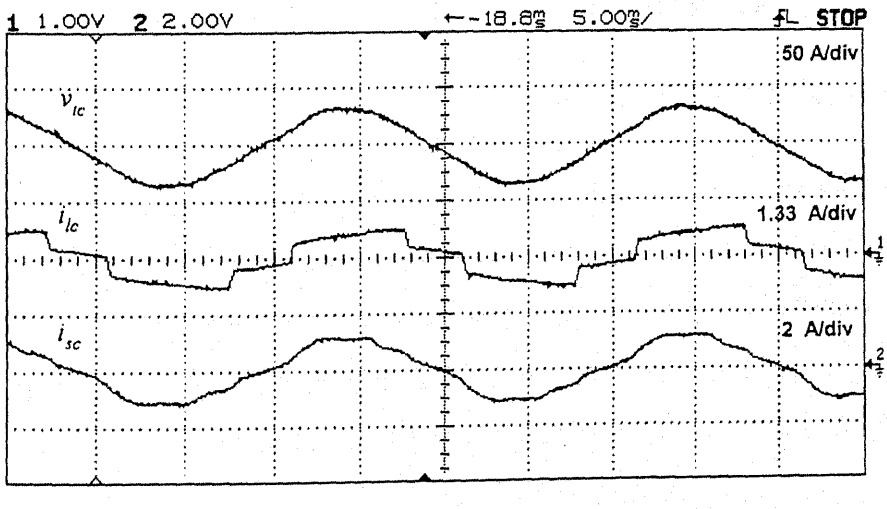


Fig. 5.40 Terminal voltage and source current in phase-*c* with state feedback controller

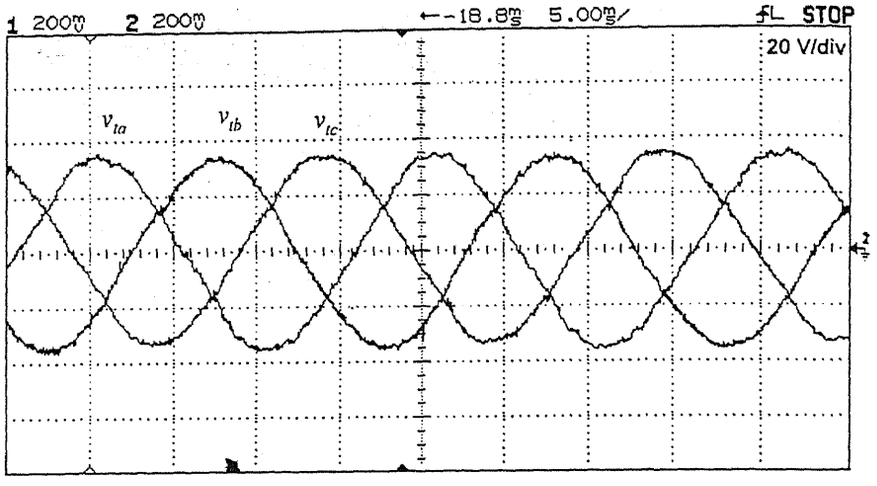


Fig. 5.41 Three-phase terminal voltages with state feedback controller

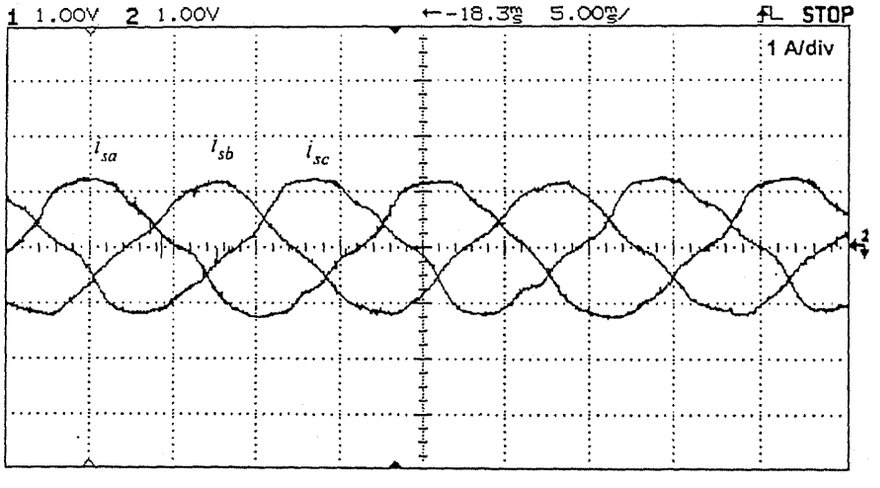


Fig. 5.42 Three-phase source currents with state feedback controller

5.6.5 Transient Performance

Ideally the compensator should take minimum time to react to the transient caused by switching of load. The settling of the compensator depends upon the time period used to compute average load power $\bar{p}_l$ and positive sequence components of terminal voltages. The minimum time period needed for averaging is half a cycle. Hence the compensator takes about half a cycle to settle to a value close to the reference.

The load current in phase-*a* is changed to only rectifier load by switching off the R-L load given in Table 5.3. The terminal voltage and load current are shown in Fig. 5.43. The terminal voltage settles within a cycle. The load of phase-*a* is now changed from rectifier load to rectifier plus R-L load and subsequently changed back to the rectifier load after two cycles. This is shown in Fig. 5.44. The corresponding source current is also shown in Fig. 5.44. It is seen that the source current settles within one cycle in each phase.

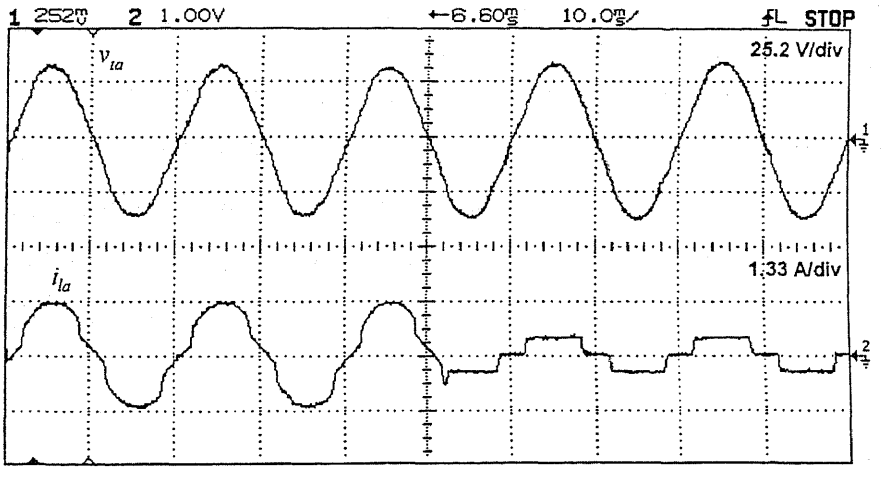


Fig. 5.43 Terminal voltage and load current transient in phase-*a*

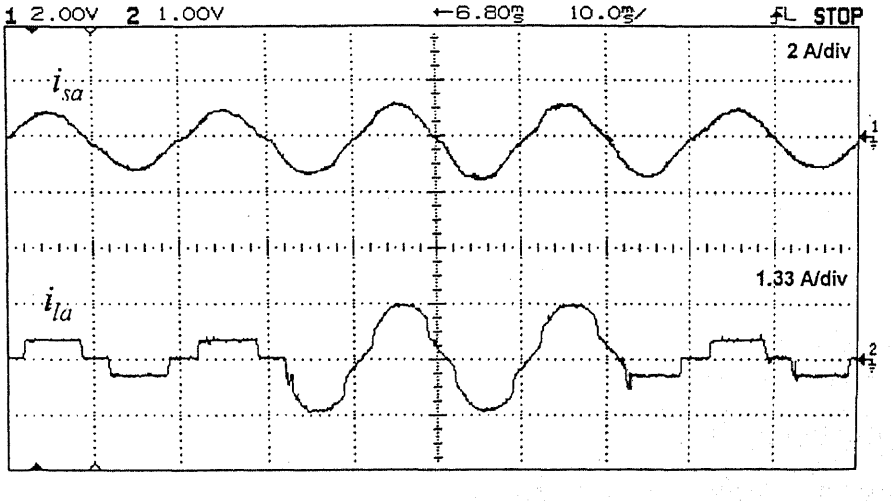


Fig. 5.44 Source current and load current transient in phase-*a*

5.7 CONCLUSIONS

Several shunt compensation schemes [43-48] are available in literature for unbalance and nonlinear load compensation. However these schemes do not give satisfactory results for supply systems supplying loads through feeders. The direct application of these shunt algorithms results in the distortion source currents and voltages at the PCC. The state feedback control of DSTATCOM, which uses shunt compensation algorithm with positive sequence extraction and filter capacitor as its part, gives however better results under non-stiff voltage source.

In state feedback control of DSTATCOM, the major issues are selection of LQR parameters, hysteresis band of control signal and selection of ac filter capacitor. The LQR parameters i.e. Q and R decide the weightage of state variables, while hysteresis band of control signal plays a vital role in deciding the switching frequency of the inverter. If the filter capacitor is small it has less smoothening effect on the source currents and PCC voltages, while large value of filter capacitor increases the current rating of inverter and the filter capacitor. The most important advantage of state feedback control is that, the switching frequency components are not directly seen in terminal voltage and source currents.

CHAPTER 6

DSTATCOM IN VOLTAGE CONTROL MODE

In the previous chapters, we have proposed various load compensation schemes that can operate with stiff or non-stiff voltage sources under balanced or unbalanced conditions to compensate unbalanced and non-linear loads. In case of unbalance in the source voltages, it was observed that this unbalance is passed on to the terminal voltages and the source currents. If the source voltages are not distorted, the compensation methods proposed in the previous chapters with state feedback controller give satisfactory results. In practice however, the upstream source voltages may be unbalanced and distorted. In such cases, the load compensation can provide satisfactory results only if PCC voltage can be made sinusoidal.

In this chapter we propose a method to operate a DSTATCOM as a voltage regulator to maintain the voltage of a specified bus. The magnitude of the bus voltage is prespecified while its phase angle is generated from the dc capacitor voltage control loop. The DSTATCOM with output filter capacitor is used in the voltage control mode. In literature, a number of papers are available on deadbeat control [81-85]. In this work, a deadbeat controller for inverter is used to regulate output voltage at PCC against distortions on the source and the load sides. The control algorithm has been discussed in detail. The proposed structure is verified through detailed simulation and experimental results.

6.1 DSTATCOM IN VOLTAGE CONTROL MODE

In a radial distribution system, the voltage of a particular bus can be distorted or unbalanced if the loads in any part of the system are distorted or unbalanced. The customers connected to a bus may be supplied by a set of unbalanced and distorted voltages, even when their loads are not contributing to pollution in the bus voltage. In this situation, a DSTATCOM can be used at this bus to clear the harmonics in the bus voltage.

Consider the three-phase four-wire radial distribution system, shown in Fig. 6.1 (a). Let us assume that we would like to correct the voltage of bus 3. The Thevenin equivalent of the system is shown in Fig. 6.1 (b). In this v_s, R_s and L_s constitute the Thevenin equivalent looking left into the network bus 3, while the equivalent load is the Thevenin impedance looking right into the network at bus 3. The only assumption involved in this is that all the loads of the distribution system are passive. We now have to use the DSTATCOM in the voltage control mode at bus 3. However, since the Thevenin equivalents can change any time depending on the load, it is desirable that these parameters are not used in the voltage controller design. Below we present a technique that only requires the timing information from the source v_{source} for synchronization.

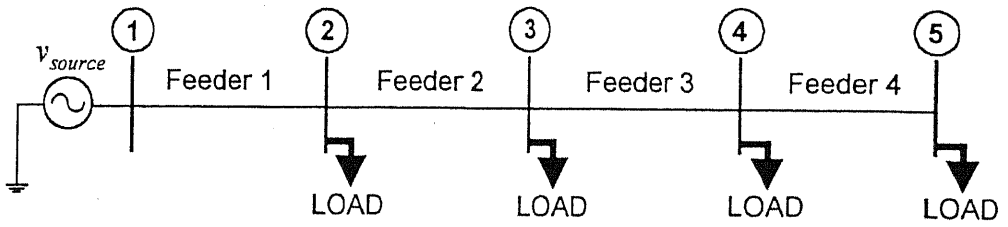


Fig. 6.1 (a) Single line diagram of a typical three-phase four-wire radial distribution system

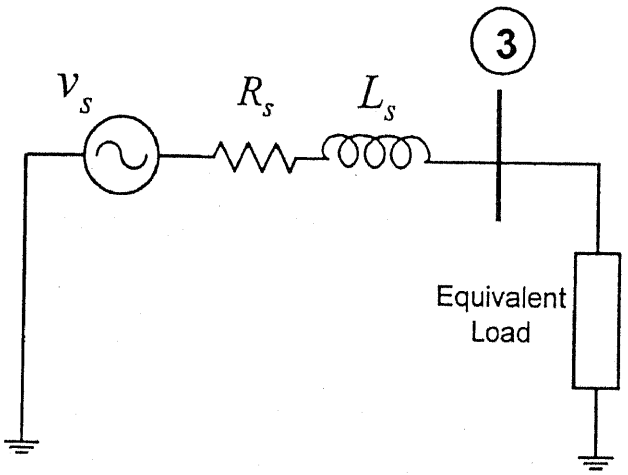
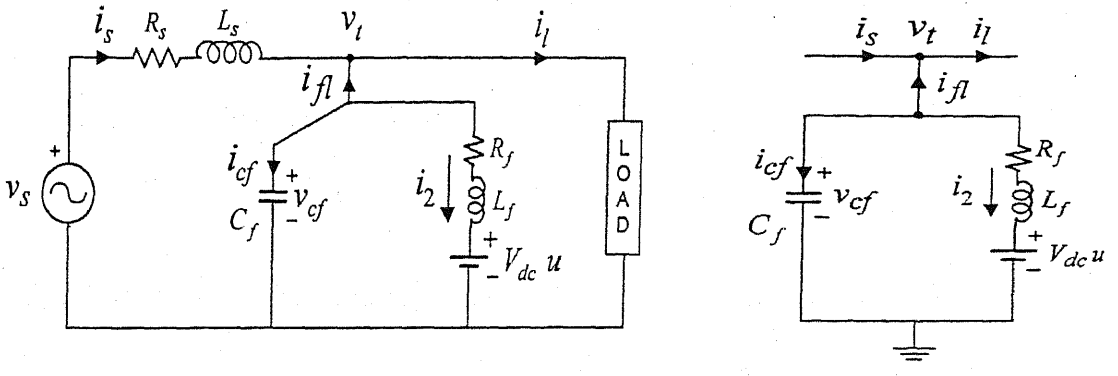


Fig. 6.1 (b) Thevenin equivalent at bus 3 of distribution system

The compensator topology used here is same as that used in Chapter 5, where a filter capacitor is used in parallel with the DSTATCOM to provide a path for the system high

frequency components. The equivalent circuit is then shown in Fig. 6.2 (a). In this we are only interested in the part of the circuit that contains the compensator. This is shown in Fig. 6.2 (b). It is assumed that it is driven by a current source i_{fl}, which is actually measurable.



(a) (b)

Fig. 6.2 (a) Compensated system equivalent circuit (b) Compensator equivalent circuit

The state space equation for the system shown in Fig. 6.2 (b) is given as,

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\,\boldsymbol{x} + \boldsymbol{B}\,\boldsymbol{u}_i \tag{6.1}$$

where $\boldsymbol{A} = \begin{bmatrix} 0 & -1/C_f \\ 1/L_f & -R_f/L_f \end{bmatrix}$ and $\boldsymbol{B} = \begin{bmatrix} 0 & 1/C_f \\ -V_{dc}/L_f & 0 \end{bmatrix}$. The state vector is given as $\boldsymbol{x}^t = [v_{cf} \;\; i_2]$ and the input vector $\boldsymbol{u}_i^t = [u \;\; i_{fl}]$.

Writing the continuous state equation (6.1) into discrete form

$$\boldsymbol{x}(k+1) = \phi\,\boldsymbol{x}(k) + \theta \begin{bmatrix} u(k) \\ i_{fl}(k) \end{bmatrix} \tag{6.2}$$

where k is k^{th} sample. The ϕ is the state transition matrix and θ is the input matrix, given by

$$\phi = e^{\boldsymbol{A}\,t_d} \text{ and } \theta = \int_0^{t_d} e^{\boldsymbol{A}\,t}\,\boldsymbol{B}\,dt$$

where t_d is the sampling period. For the system of (6.1) let us define the elements of these matrices as

$$\phi = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} \text{ and } \theta = \begin{bmatrix} \theta_{11} & \theta_{12} \\ \theta_{21} & \theta_{22} \end{bmatrix} \tag{6.3}$$

We can then write (6.2) as

$$v_{cf}(k+1) = \phi_{11}\, v_{cf}(k) + \phi_{12}\, i_2(k) + \theta_{11}\, u(k) + \theta_{12}\, i_{fl}(k) \tag{6.4}$$

Let $v_{t\,ref}$ be the reference (nominal) voltage to be maintained at the terminal bus. Let us now choose a cost function as

$$J = [v_{cf}(k+1) - v_{t\,ref}(k+1)]^2 \tag{6.5}$$

To minimize the cost function we take its derivative with respect to $u(k)$ and equate it to zero, i.e.,

$$\frac{\partial J}{\partial u(k)} = 2\left[v_{cf}(k+1) - v_{t\,ref}(k+1)\right] \frac{\partial v_{cf}(k+1)}{\partial u(k)} = 0 \tag{6.6}$$

The quantity $\dfrac{\partial v_{cf}(k+1)}{\partial u(k)} = \theta_{11}$ is not zero. Therefore $v_{cf}(k+1) = v_{t\,ref}(k+1)$ for the minimum J. Using this fact and (6.4), the control input $u(k)$ is given by

$$u(k) = \frac{v_{t\,ref}(k+1) - \phi_{11} v_{cf}(k) - \phi_{12} i_2(k) - \theta_{12} i_{fl}(k)}{\theta_{11}} \tag{6.7}$$

The minimization of the cost function of (6.5) results in a control action that takes a corrective measure based on the knowledge of reference voltage at the next sampling instant. This control is termed as a deadbeat control.

6.1.1 Switching Control

Once the control signal $u(k)$ is obtained from the deadbeat controller, the switch control law is obtained in the same manner as described in Chapter 5 Sub-section 5.4.2. This is given by (Fig. 6.3),

$$\begin{aligned} &\text{if } u(k) > \lim \text{ then } S = 1, \bar{S} = 0 \\ &\text{else if } u(k) < -\lim \text{ then } S = 0, \bar{S} = 1 \end{aligned} \tag{6.8}$$

The selection of the parameter lim determines the switching frequency as in a hysteresis band current control.

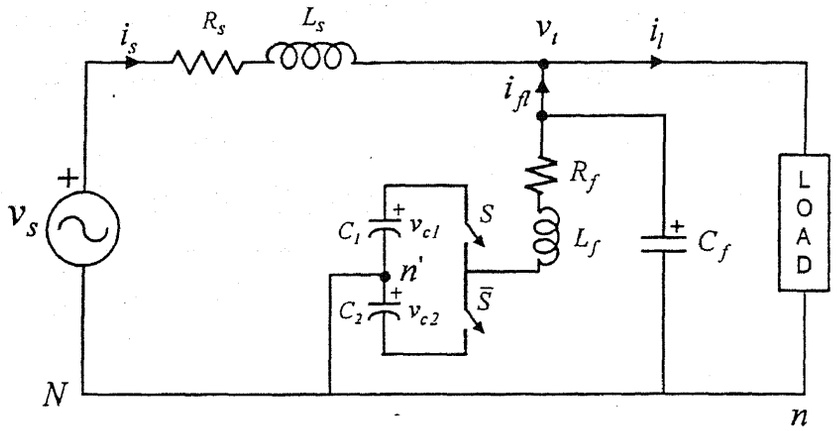


Fig. 6.3 Neutral clamped inverter topology of DSTATCOM in voltage control mode

6.1.2 Reference Voltage Generation

In Fig. 6.3, it is assumed that two rectifiers supply dc capacitors. In this situation, power sharing between the source and the inverter is not in our control. If the terminal voltage and the source voltage are synchronized with their phase and zero crossings matching, the phase angle between the terminal and source voltage is zero. It implies that the entire real power supplied to the load will come from the inverter. Thus the rating of the inverter, transformers and rectifiers supplying the inverter will considerably increase. This is certainly not desirable, as the source should supply the load directly. In addition, the source should also supply the inverter losses. To facilitate proper power sharing, the phase angle between the source and terminal voltage must be properly set. This can be done in open loop. However this is not a desirable scheme, as this angle will change with the changes in the load power.

Below we propose a scheme in which we decide the angle of the bus voltage v_t, in a closed loop – from the dc capacitor voltage control. It is assumed that rectifiers are not used to supply the dc capacitors.

As discussed in the previous chapters some real power should be drawn from the source towards the dc link to maintain the total voltage across dc capacitors. The capacitor voltage control scheme is now used to generate the phase angle of the ac bus voltage such that inverter losses are supplied by the source. Here we assume that the magnitude of the terminal (PCC) voltage is pre-specified and its angle is obtained from the closed loop. The block diagram of this control scheme is shown in Fig. 6.4. It has two control loops. The outer control loop is dc capacitor voltage control loop and inner loop is the δ control loop.

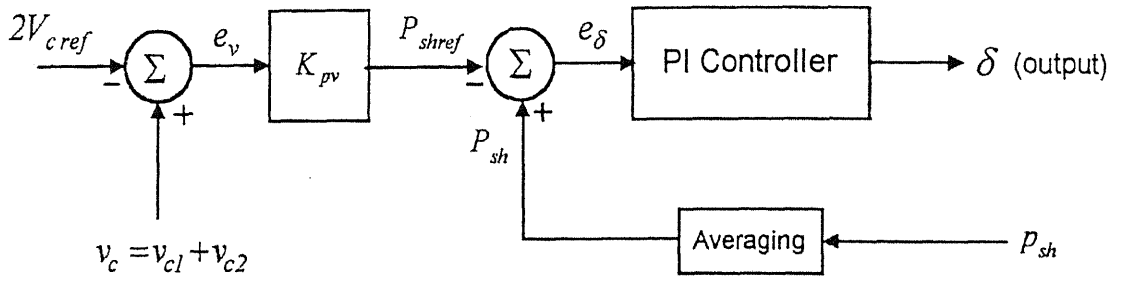


Fig. 6.4 Block diagram of closed loop voltage control

As mentioned earlier, the deviation of the total capacitor voltage from its reference value ($2V_{cref}$) is a good indication of losses in the inverter. We add the two capacitor voltages and compare with the reference value. This is done only once per cycle. It is to be noted that the dc capacitor voltage usually contains the switching frequency components. Therefore, comparing its instantaneous value with that of the reference will result in large error in control. Instead, the average value of the dc capacitors can be considered. Alternatively, we can choose the value of the capacitor voltage at the end of a cycle and try to regulate it around a reference value. We use a proportional controller with a gain of K_{pv} rather than a PI controller used in the earlier chapters. The proportional controller generates a signal P_{shref}, which indicates the amount of power that must be drawn from the source in order to maintain the dc capacitor voltage. We can thus write,

$$P_{shref} = K_{pv}(v_c - 2V_{cref}) \tag{6.9}$$

Since the loop maintains the capacitor voltage, we call it the outer voltage loop.

The power angle δ (which is a phase angle between terminal and source voltage in their respective phases) is computed in such a way that it ensures that the shunt link draws an amount of power (P_{sh}) that is equal to P_{shref}. To achieve this a PI controller is used. The output of the controller is power angle δ. This is given as

$$\delta = K_{p\delta}(P_{sh} - P_{shref}) + K_{i\delta}\int (P_{sh} - P_{shref})dt \tag{6.10}$$

where K_{p_δ} and K_{i_δ} are the PI controller gains. These gains are chosen very carefully through trial and error. High gain may cause unnecessary oscillations and may even cause instability.

The instantaneous actual power in shunt link p_{sh} is computed as follows.

$$p_{sh} = v_{ta}i_{fla} + v_{tb}i_{flb} + v_{tc}i_{flc} \tag{6.11}$$

Again the instantaneous value of this power does not give any indication of the real power into or out of the inverter. The average value of p_{sh} on the other hand is more meaningful. Therefore the instantaneous samples are stored and at the end of cycle the average value of these samples are computed. This average value of actual shunt power is denoted by P_{sh} and is used in implementing the inner power loop or δ control loop.

The angle δ is defined with the source voltage as reference. Thus we require the zero crossing of the phase-*a* voltage of the source. In a laboratory set-up, this does not cause any problem. However, in an actual practical installation, we assume that this data is telemetered. Once we assume that this data is obtained, the reference voltage for the PCC bus are given as,

$$\left.\begin{aligned} v_{t\,refa} &= V_{t\,refm}\sin(\omega t - \delta) \\ v_{t\,refb} &= V_{t\,refm}\sin(\omega t + 2\pi/3 - \delta) \\ v_{t\,refc} &= V_{t\,refm}\sin(\omega t - 2\pi/3 - \delta) \end{aligned}\right\} \tag{6.12}$$

where $V_{t\,refm}$ is the peak of desired PCC voltage.

6.2 SIMULATION RESULTS

In this section, detailed simulation results have been presented. It has been demonstrated that DSTATCOM in voltage regulator mode is able to maintain the terminal bus voltage at the nominal value irrespective of the load changes and upstream voltage fluctuations. When there are transients on the load side, terminal voltage is still maintained at the nominal value. The dc capacitors are initially charged to the reference voltage (V_{cref}) with switch S_f open in Fig. 6.5. The power angle δ is assumed to have an initial value of zero. Before DSTATCOM is connected to the PCC bus, the voltage source inverter is run independently to construct three-phase voltages (across ac filter capacitors) equal to $v_{t\,ref}$ (6.12). When DSTATCOM is connected to the PCC bus by closing switch S_f, the dc capacitor voltage control loop is activated. The simulation parameters are given in Table 6.1.

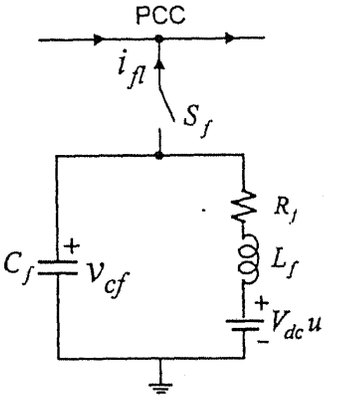


Fig. 6.5 DSTATCOM connection to the PCC bus

Table 6.1 System Parameters

System voltages: 360V ±10% (peak), sinusoidal and may contain harmonics and exhibit swell, sag
Feeder impedance: Z_s = 1 + j 3.14 Ω
Terminal bus nominal voltage: 360V (peak), sinusoidal and balanced
DC capacitors (C_1 , C_2)**:** 2200 μF each
Interface inductors (L_{fa}, L_{fb}, L_{fc})**:** 20 mH, 0.2 Ω
AC capacitors (C_{fa}, C_{fb}, C_{fc})**:** 50 μF in each phase
Voltage controller gains of dc capacitor loops: K_{pv}=10
δ **control loop gains:** $K_{p\delta}$ = 4e-6, $K_{i\delta}$ = 8e-6
Reference value of dc capacitor voltages: 600 V each capacitor
Control signal hysteresis band for each phase: lim = 1

The three-phase load consists of:

- $Z_a = 40\ \Omega, Z_b = 50\ \Omega, Z_c = 72 + j\ 84\ \Omega$
- Three phase diode bridges rectifier drawing a current of 5 A

Fig. 6.6 shows the results before DSTATCOM is connected to the bus i.e. S_f is open (Fig. 6.5). The source voltages are shown in Fig. 6.6 (a) and the load currents are shown in Fig. 6.6 (b) respectively. Without any regulation the terminal voltages are shown in Fig. 6.6 (c). We see in Fig. 6.6 (c) that terminal voltages contain the spikes due to diode rectifier load and feeder inductance. In Fig. 6.6 (d), the voltages across ac filter capacitor voltages are shown. These are sinusoidal and balanced with a voltage of 360 V peak.

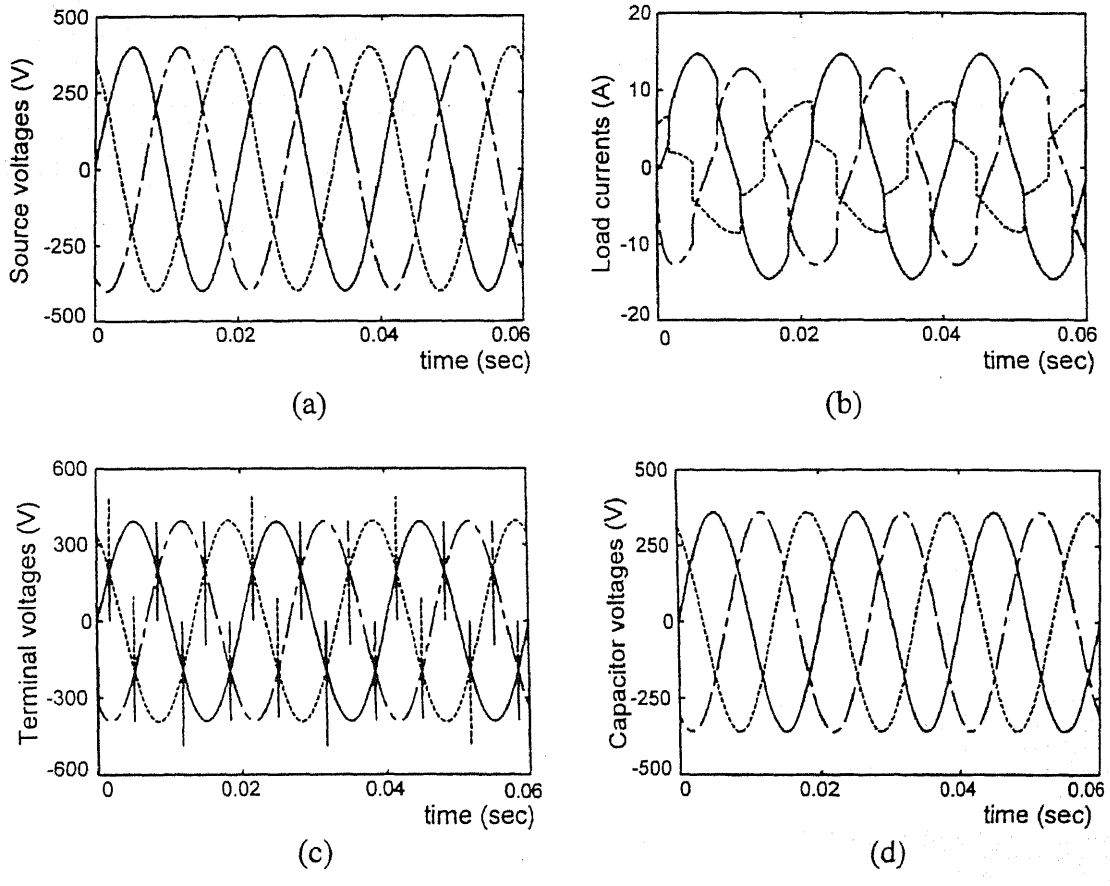


Fig. 6.6 (a) Source voltage (400 V peak) (b) Load currents for unbalanced and rectifier load (c) Terminal voltage (d) Filter capacitor voltage before DSTATCOM connection to the PCC bus

6.2.1 Performance in Case of Over Voltages

The source voltages are balanced sinusoids with 400 V (peak) as shown in Fig. 6.6 (a). The DSTATCOM is connected to the terminal bus at the end of one cycle and the total voltage of dc capacitors is regulated using closed loop control scheme as discussed in Sub-section 6.1.2. The phase-*a* terminal bus (v_{ta}) and the filter capacitor voltage (v_{cfa}) in phase-*a* are shown in Fig. 6.7 (a). It can be seen that the difference between these voltages is not significant for this load (except spikes in terminal voltage) and after connecting DSTATCOM to the bus, the two voltages become the same. The phase-*a* voltage is sinusoidal except for the small ripple due to inverter switching that can be seen in the waveform. Since the terminal voltages are balanced and so are the source voltages, as can be seen in Fig. 6.7 (b).

The variation of δ is shown in Fig. 6.7 (c). The initial value of δ is assumed to be zero and is updated in every cycle. The variation of capacitor voltages is shown in Fig. 6.7 (d). As soon as the DSTATCOM is connected to the PCC, the PI controller starts increasing the value of δ. To the DSTATCOM it means that the load requires more power that can not be immediately supplied by the source. It therefore transiently supplies this power resulting in discharge of dc capacitors. However the control action soon brings this voltage back to the reference value by bringing δ to settle at the steady state value. The overshoot remains for about 10 cycles and during this duration more power is drawn from the source to sustain the total voltage across dc capacitor voltage.

The reference shunt power P_{shref} and the actual shunt power P_{sh}, when averaged over a cycle are shown in Fig. 6.8 (a) while P_{shref} and instantaneous actual shunt power p_{sh} are plotted in Fig. 6.8 (b). It is seen from Fig. 6.8 (a) that P_{sh} tracks P_{shref}. Furthermore, this can also be seen from Fig. 6.8, where P_{shref} is the average of instantaneous shunt power, p_{sh}.

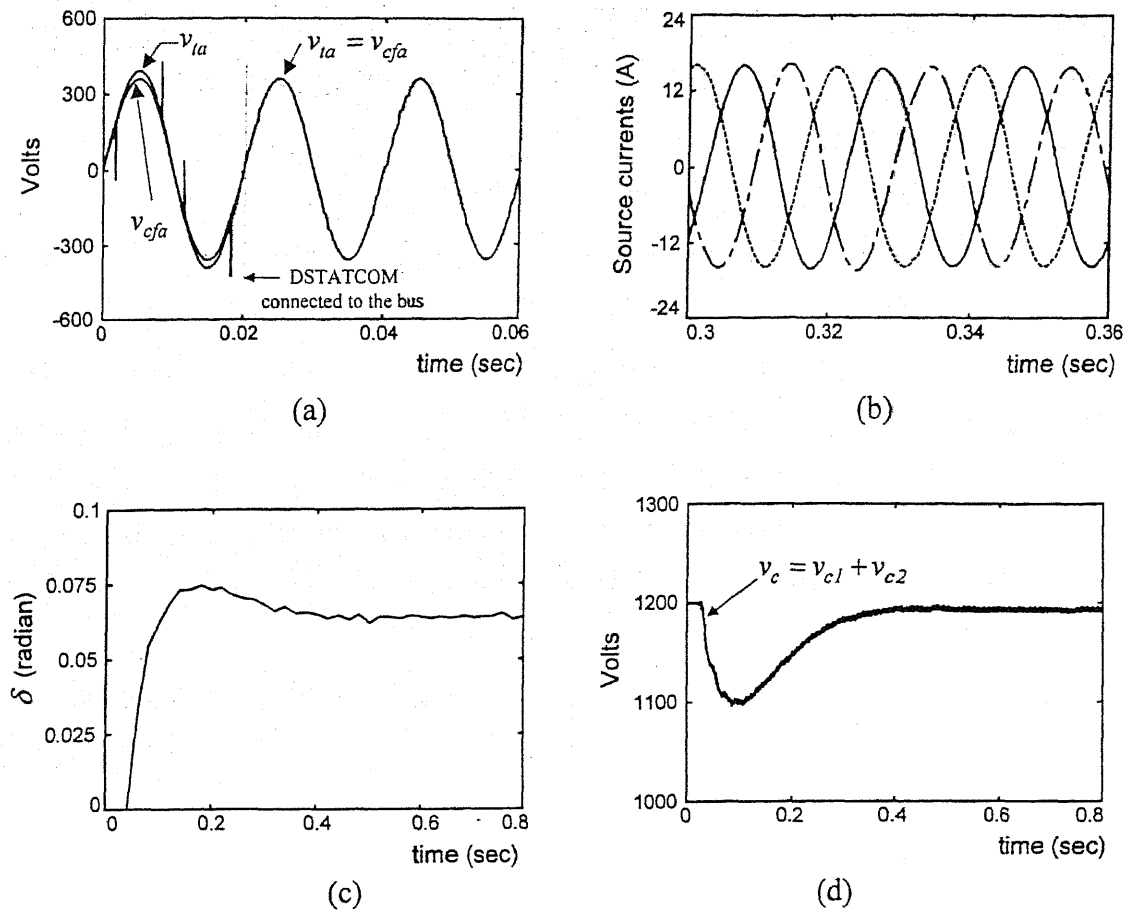


Fig. 6.7 (a) Terminal voltage and filter capacitor voltage in phase a (b) Steady state source currents (c) Variation of δ (d) Total voltage across dc capacitors

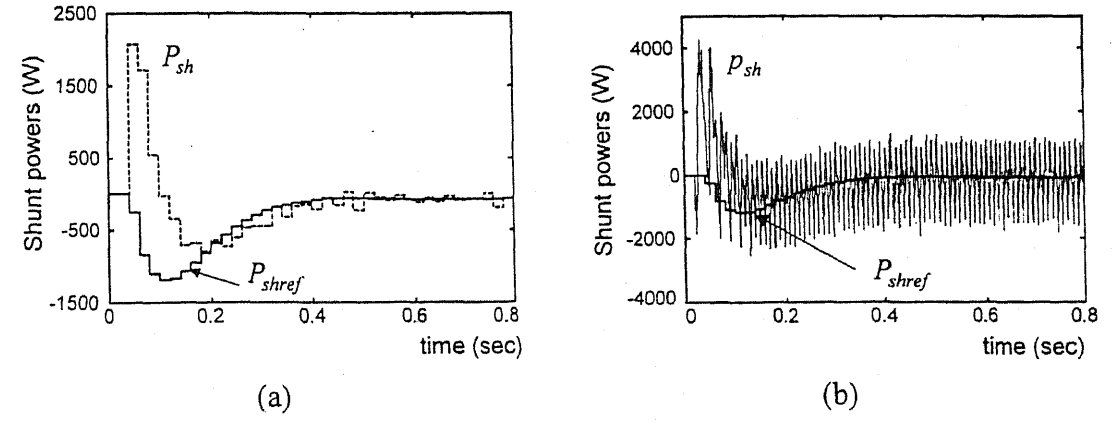


Fig. 6.8 (a) Reference and actual shunt power averaged over cycle (b) Reference shunt and actual instantaneous shunt power

6.2.2 Performance in Case of Under Voltages

The source voltages are assumed to 324 V peak in each phase. The terminal voltages are regulated to the nominal value of 360 V peak. The load configuration is same as given in Table 6.1. The variation of power angle is shown in Fig. 6.9 (a). The initial value of δ is taken as 0.091 radian. It is seen that in under voltages the power angle settles to a higher value 0.16 radian (9.2°) than the previous case. Since the terminal voltage is to be regulated at nominal value and loads are same, the power angle must be raised to supply the same power to the load. The terminal voltages are shown in Fig. 6.9 (b). It is observed from the figure that during the first cycle, when DSTATCOM is connected to the bus, the peak terminal voltages are below the peak of source voltages due to drop in the feeder. As soon as DSTATCOM in voltage control mode operates, the terminal voltages are brought to the nominal values. The shunt power and dc capacitor voltages are shown in Fig. 6.9 (c) and (d) respectively.

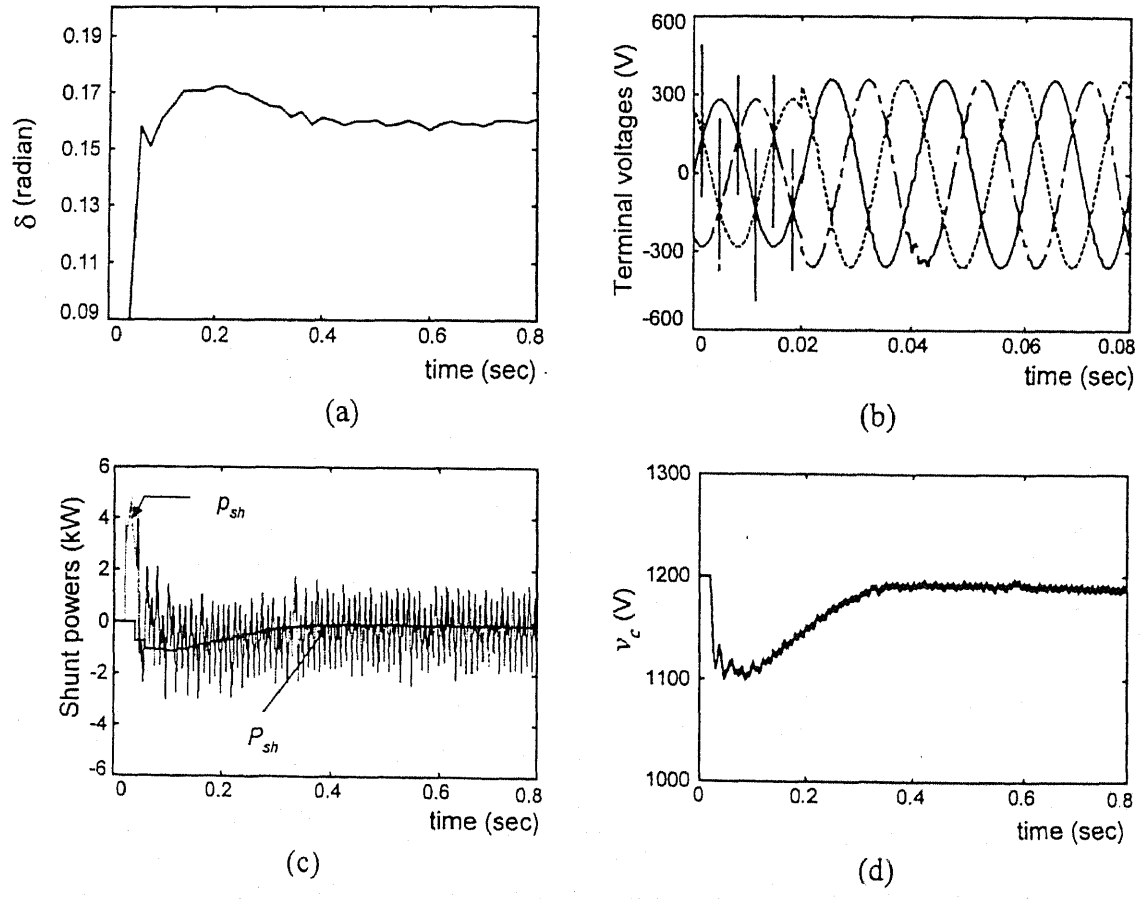
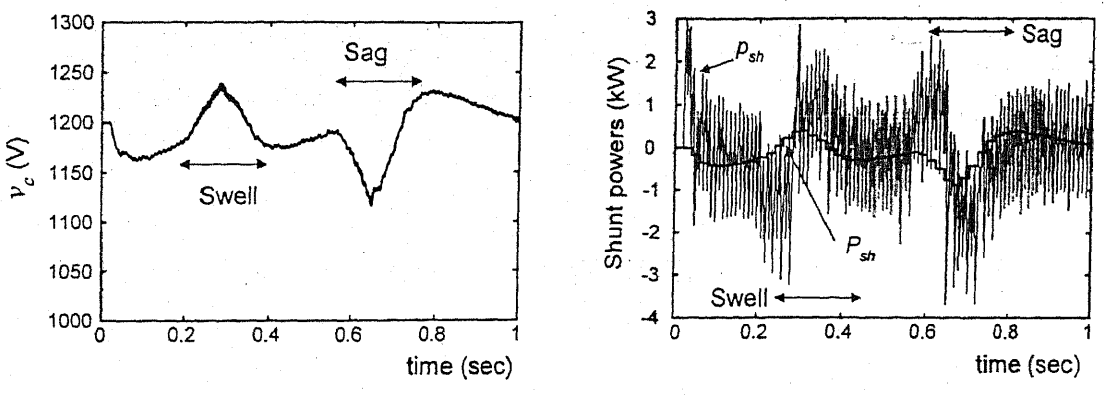


Fig. 6.9 (a) Power angle variation (b) Terminal voltages (c) Shunt powers (d) Total dc capacitors voltage

6.2.3 Performance in Case of Voltage Swell and Sag

Voltage swell and sag are actually special (transient) cases of over and under voltage respectively. The short duration (a few cycles) transient over voltage is called a swell while an under voltage is called a sag. The voltage swell and sag in source voltage is shown in Fig. 6.10 (a). The DSTATCOM is operated in the voltage control mode. The terminal voltage of phase-*a* after compensation is shown in Fig. 6.10 (b). It is seen that terminal is regulated to nominal value i.e. 360 V, peak against the transient changes in the source voltage. The terminal voltage on magnified time scale is shown in Fig. 6.10 (c). The figure indicates that the terminal voltages are balanced and sinusoidal. Fig. 6.10 (d) and (e) show the power angle and total dc capacitor voltage (v_c). It is seen from the Fig. 6.10 (d) that initially for 10 cycles during which the source voltages are nominal voltages, the power angles settles at 0.092 radian (5.3°).

In the next 8 cycles there is a voltage swell of 20% from the nominal value. As a result of this, the power angle decreases and settles at 0.066 radian (3.8°). During the voltage swell, there is rise in v_c (Fig. 6.10 (e)), because swell is a temporary phenomenon and sufficient time for settling δ is not available. For the next 10 cycle, the source voltages again become nominal value and δ settles to δ_o which is 0.092 radian (5.3°). The voltage v_c settles to $2V_{dcref}$. Later on voltage sag (20% fall from the nominal value) occurs. Due to fall in the level of source voltage, power angle increases to 0.15 radian (8.6°) to ensure same power transfer to the load at nominal terminal voltages. The voltage v_c falls as control loop takes some time to settle at higher value of δ. Again when the voltage sag is over δ settles to δ_o and v_c settles to $2V_{dcref}$. The reference shunt power P_{shref} and instantaneous shunt power p_{sh} are plotted in Fig. 6.10 (f). During the voltage swell the P_{shref} increases while during voltage sag P_{shref} decreases. The actual shunt power p_{sh} tracks P_{shref} to ensure desired power flow from the source to the load and to supply losses in the inverter.



(e) (f)

Fig. 6.10 (a) Swell and sag in source voltage (b) Terminal voltage (c) Terminal voltage magnified (d) Variation of δ (e) Total dc capacitor voltage (f) Reference shunt power and instantaneous actual shunt power

6.2.4 Performance when Source Voltages are Unbalanced and contain Harmonics

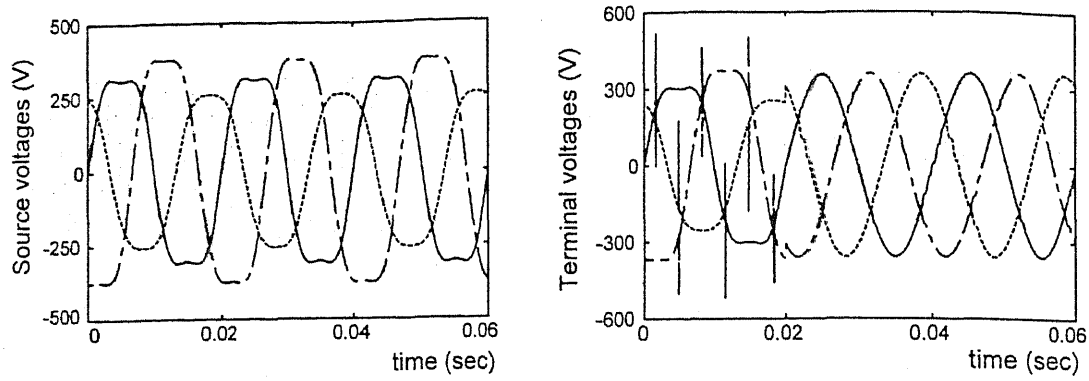
The DSTATCOM voltage control mode must be able to clean up any supply side disturbances. To investigate this, we choose a source voltage that is both unbalanced and distorted. The three-phase source voltages are given by

Phase-*a*: 360 V (peak) and 15% 3rd harmonic

Phase-*b*: 432 V (peak) and 16% 3rd harmonic

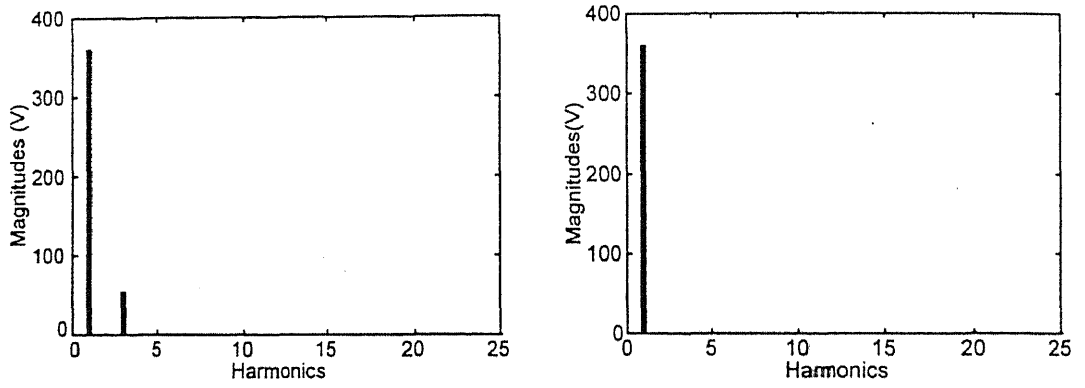
Phase-*c*: 288 V (peak) and 8% 3rd harmonic

These source voltages are shown in Fig. 6.11 (a). The terminal voltages before regulation and after regulation are shown in Fig. 6.10 (b). The improvement in the terminal voltage after the connection of the DSTATCOM is evident. The power angle settles around 0.1 radian, i.e. 5.7°. The harmonic spectrum of source voltage and terminal voltage in phase-*a* are shown in Fig. 6.11 (a) and (b) respectively. The THD in v_{sa} is 15% and that in v_{ta} after regulation is 0.95%.



(a) (b)

Fig. 6.11 (a) Unbalanced source voltages with harmonics (b) Terminal voltages before and after regulation



(a) (b)

Fig. 6.12 Harmonic spectrum in (a) source voltage (b) Terminal voltage after regulation

6.2.5 Performance when Load Transient Occurs

We investigate the effect of abrupt changes in load on the performance of DSTATCOM in voltage control mode. The load pattern is divided into four regions.

Region 1: The load is normal and is same as given in Table 6.1. The load current in each phase is the sum of current due to R-L load and rectifier current in respective phases. This load gives normal load current.

Region 2: R-L load is removed in all phases thus only rectifier load is present. This reduces load current in each phase considerably.

Region 3: R-L load in each phase is halved retaining same rectifier load, thereby making load current larger than the normal load current.

Region 4: The load again become normal and so are load currents.

These four regions showing abrupt load current changes are shown in Fig. 6.13.

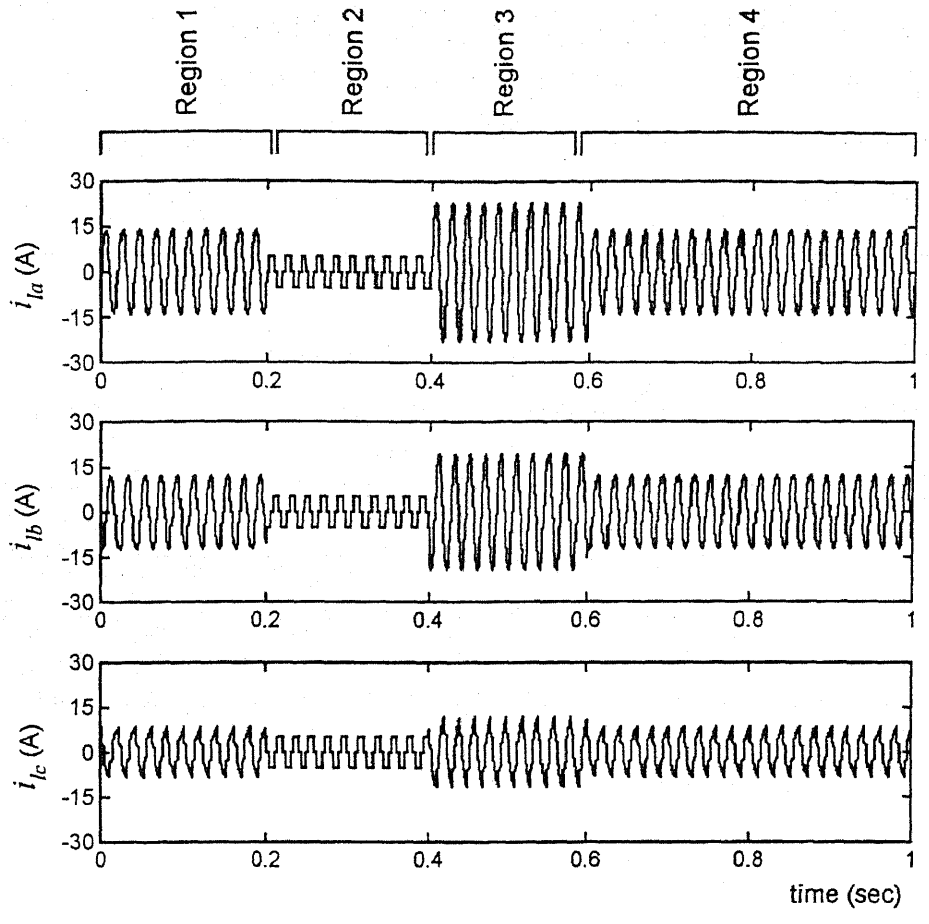


Fig. 6.13 Transient in load currents

For region 1, the load is normal and the power angle δ settles around 0.09 radian. The total dc capacitors voltage v_c is maintained at 1200 V, which is total reference voltage. In region 2 where unbalanced R-L load is removed from all three phases. Only diode rectifier current of magnitude 5 A, is present. Thus due to smaller load currents than normal currents δ is reduced to smaller value than that for a normal load. As seen from Fig. 6.14 (a), its value is 0.027 radian (1.6°). From Fig. 6.14 (b) it is also seen that v_c approaches towards $2V_{dcref}$. In region 3, the load suddenly rises and therefore power angle begins to rise and settles around 0.16 radian (9.16°), while v_c drops transiently and approaches towards $2V_{dcref}$. After that the load is switched to normal value as indicated by region 4 in Fig.

6.13, the δ shows a fall and settles to 0.09 radian (5.1°), while v_c settles to its reference value i.e. $2V_{dcref}$ as seen from Figs. 6.14 (a) and (b) respectively. It is to be noted that the total capacitor voltage in region 2 and 3 tries to recover to the reference value but the load is changed in either case before it can reach the steady state. It is also mentioned that for the parameters considered in simulation, the switching frequency of the inverter is approximately 3 kHz.

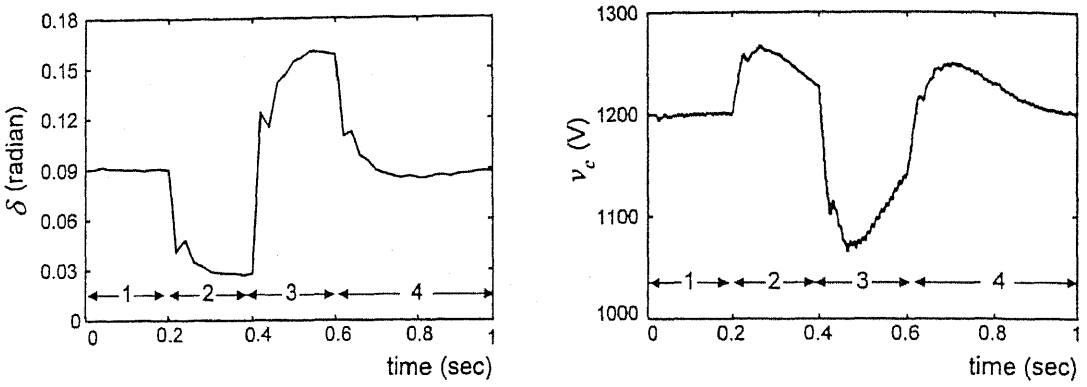


Fig. 6.14 (a) Variation of δ (b) Total dc capacitor voltage under transient load conditions

6.3 CONNECTING DSTATCOM TO THE PCC BUS

The DSTATCOM in voltage control mode is an important voltage source. Therefore connecting of the DSTATCOM to the PCC bus is an important issue. It can easily be seen that this can not be done arbitrarily. The voltage difference between the PCC bus voltage and the voltage across the filter capacitors can cause severe transient in the system. Therefore, we must close the connecting switch S_f shown in Fig. 6.5, when the two voltages are nearly equal. The following steps are taken to connect the DSTATCOM to the PCC bus.

1. Initially dc capacitors are supplied separately through independent rectifiers and switch S_f (Fig. 6.5) is open implying that $P_{sh} = 0$ as $i_{fl} = 0$ as per (6.11). Since the voltages across the dc capacitors are not to be controlled and $P_{sh} = 0$ as $i_{fl} = 0$, the outer dc capacitor voltage control loop is not activated at this point of time. In this condition, the source supplies the load power and the switching losses are supplied by the rectifiers, feeding the dc capacitors. Thus in Fig. 6.4, $P_{sh} = 0$, $P_{shref} = 0$ and $\delta = 0$ in (6.12). The

magnitude of the output voltage of the inverter, i.e. the voltage across ac capacitors is the desired bus voltage. It is assumed that the difference between rms values of the actual PCC and the desired PCC voltage is small so that the switch S_f in Fig. 6.5 can be closed and the resulting charging/discharging capacitor current is not excessive. This assumption is made in order to simplify the procedure for connecting the ac filter capacitors to the PCC.

2. Now the ac filter capacitors are connected to the terminal bus by closing switch S_f in Fig. 6.5. The inner δ control loop now raises the angle δ to the value required for making P_{sh} equal to zero. During this phase, the inverter losses are supplied by the independent rectifiers. The load power adjusts to a new value corresponding to v_{tref}. The transient in P_{sh} also causes power flow between the rectifiers feeding dc capacitors and the bus.
3. In the third step, the dc capacitors are disconnected from the rectifier and the outer dc capacitor voltage control loop is activated. The net effect is that the loop increases the steady state value of δ, so that the source supplies the load power as well as losses in the inverter.

6.4 EXPERIMENTAL RESULTS

The experimental system parameters are given in Table 6.2.

Table 6.2 Experimental system parameters

System voltages: 36V (peak) sinusoidal and may contain distortion
Feeder impedance: Z_s = 1+j3.14 Ω
DC capacitors (C_1 , C_2)**:** 2200 μF each
Interface inductors (L_f)**:** 20 mH, 2 Ω
AC capacitors (C_f)**:** 50 μF in each phase
Voltage controller gains of dc capacitor loops: K_p=1.0, K_i=0.01.
Delta control loop gains: K_{pv}=1, $K_{p\delta}$ = 0.0001, $K_{i\delta}$ = 0.001.
Reference value of total dc capacitor voltage: 90 V
Control signal hysteresis band: lim = 0.1

Three-phase voltage of the filter capacitors, $v_{cfa}, v_{cfb}, v_{cfc}$ similar to v_{cf} in Fig. 6.2 (a) are obtained using Hall effect voltage transducers. In addition to this, we employ Hall effect current transducers for the measurement of filter capacitor currents, i_{cfa}, i_{cfb}, i_{cfc} similar to i_{cf}, in Fig. 6.1 (a), shunt link currents $i_{fla}, i_{flb}, i_{flc}$ similar to i_{fl} in Fig. 6.1 (a). These quantities are obtained in IBM compatible PC (P-II, 350 MHz), through data acquisition card (NuDAQ 9118DG). Detailed connection of the voltage and current transducers are given in Appendix A.

6.4.1 Balanced Resistive Load Only

The load consists of resistors that have 50 Ω resistance in each phase. The source voltage and terminal voltage in phase-*a* are shown in Fig. 6.15. It is seen that the terminal voltage is regulated near the source voltage however the terminal voltage (v_t) lags the source voltage (v_s) in each phase by t_δ which corresponds to 7.5°. This is also verified by δ plot in Fig. 6.16 as steady state value of δ (δ_{ss}) is 0.13 radian. The delta angle is small because the load draws a small, balanced current from each phase. The filter capacitors are connected to the bus at $t = t_{con}$. The δ control loop is activated at $t = t_{\delta on}$ immediately followed by switching off the rectifier supply to dc capacitors.

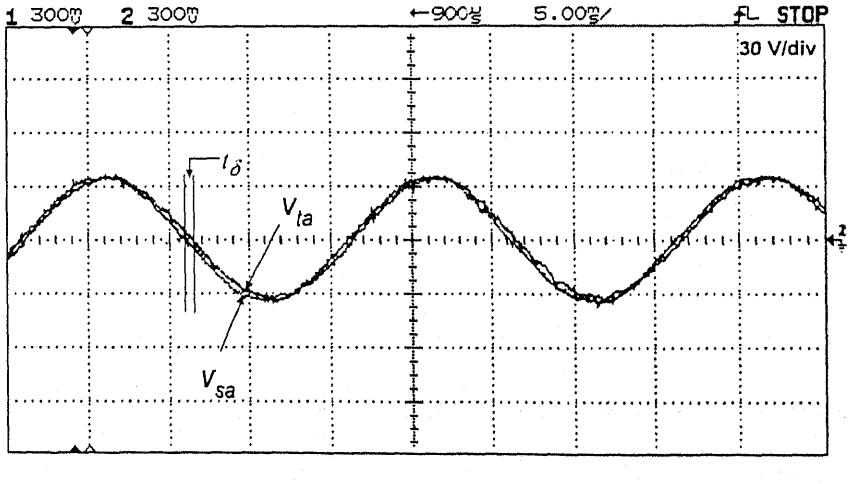


Fig. 6.15 Source voltage and terminal voltage in phase-*a*

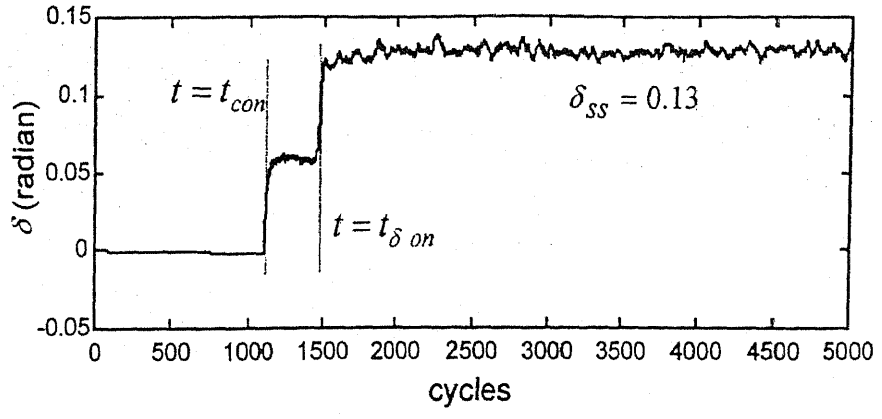


Fig. 6.16 Variation of δ

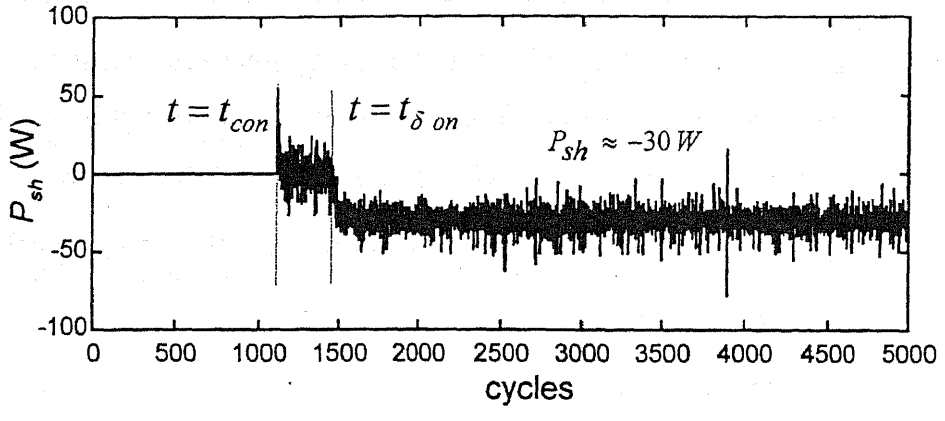


Fig. 6.17 Variation of power in shunt link

In Fig. 6.16, δ is initially zero before the DSTATCOM is connected to the terminal bus. The corresponding shunt power is zero as shown in Fig. 6.16. Now the DSTATCOM is connected $t = t_{con}$ by closing switch S_f in Fig. 6.5. While this switch is closed, P_{shref} is set to zero in the program indicating that rectifiers are supplying the dc capacitors. However, there is some value power angle $\delta = 0.06$ radian, needed to supply the load drawing small currents from each phase. Later on at $t = t_{con}$, the δ control loop is activated. At the same time the rectifiers supplying two dc storage capacitors are disconnected. Now, the source supplies the load as well as power losses in the inverter. It is seen from Fig. 6.16 that δ increases for the above reason. It settles around 0.13 radian, which corresponds to 7.5°.

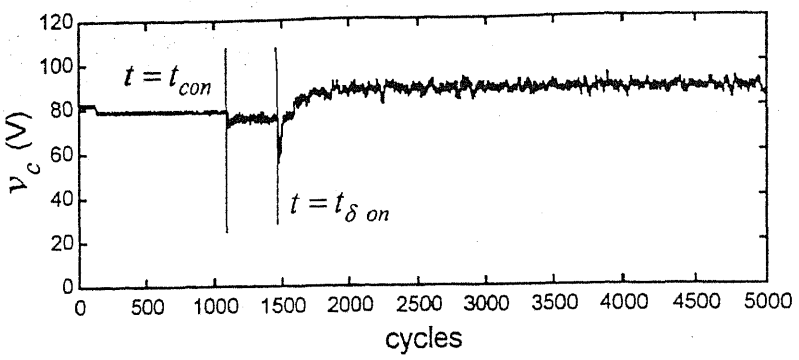


Fig. 6.18 Variation of total dc capacitor voltage

Fig. 6.18 shows the variation of the total capacitor voltage (v_c). Initially, each dc capacitor voltage is pre-charged to 40 V each, thus the total voltage across dc capacitors is 80 V. The dc capacitors are pre-charged using two rectifiers supplied by single phase ac source. At point $t = t_{con}$, the rectifiers are loaded and the v_c reduces slightly from 80 V. Later at $t = t_{con}$, closed loop δ control is activated and the rectifiers are switched off. It is seen that there is a small dip in v_c. This is because of the fact that since the dc capacitors are no longer supplied from the rectifiers through ac source. To retain the total voltage of the capacitors to a constant value the inverter power must be supplied from the source. It is seen from Fig. 6.17 that this real power transfer does not take place immediately. It takes some time for source to supply the full inverter losses that is approximately 30 W. During this time the capacitor supplies the inverter losses at the expense of a dip in their voltages. The δ control loop regulates the total dc capacitor voltage to 90 V. If the voltage dip is significant, it may result in distortions in terminal voltage especially if dc capacitor voltage is below the peak of the terminal voltage. This may not be desirable if sensitive loads are connected across the terminal bus. To overcome the above problem, the supply of dc capacitor is not switched off immediately after the activation of δ control loop. The dc capacitors are switched off when source is already supplying the inverter losses as a result of δ control loop. In the Fig. 6.19, the δ control loop is activated at 1550^{th} cycle. Between cycles 1550 and 2315 the source is ready to supply inverter losses due to action of δ control loop. The supply to dc capacitors is switched off at 2316^{th} cycle. The voltage dip in v_c is thus avoided.

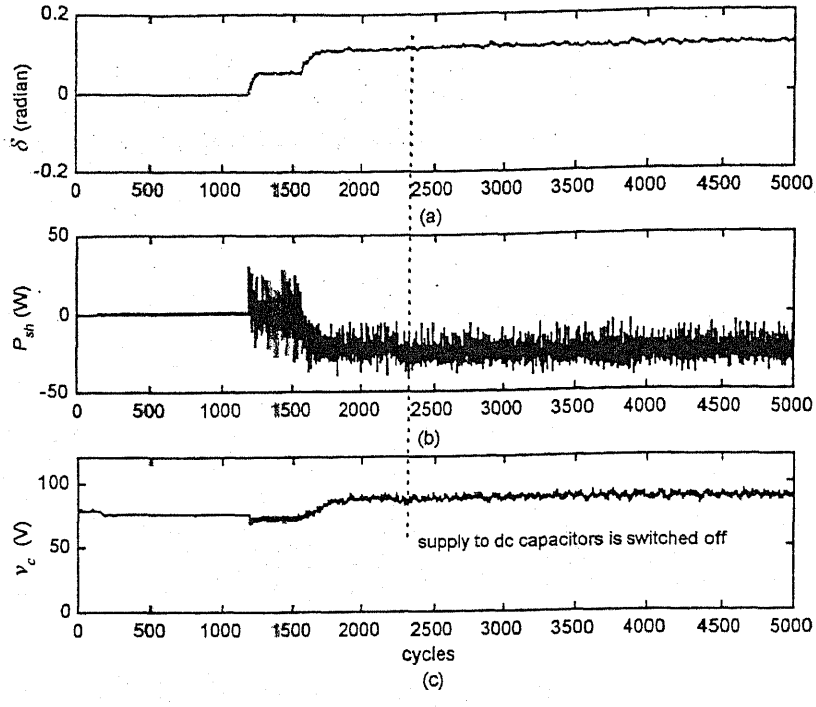


Fig. 6.19 Variation of (a) δ (b) P_{sh} and (c) v_c

6.4.2 Purely Non-linear Load

A three-phase full bridge diode rectifier is now considered as the only load. It draws a dc current of 0.5 A from the source in each phase. The various voltage waveforms are shown from Fig. 6.20 to Fig. 6.22 while δ and P_{sh} are shown in Fig. 6.23 (a) and (b) respectively.

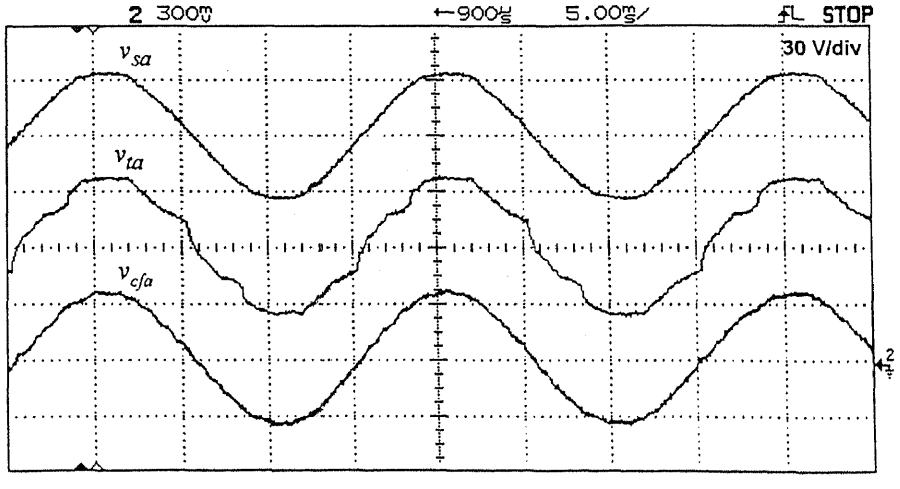


Fig. 6.20 The voltages waveforms of source, terminal, and ac capacitor before connecting DSTATCOM to PCC

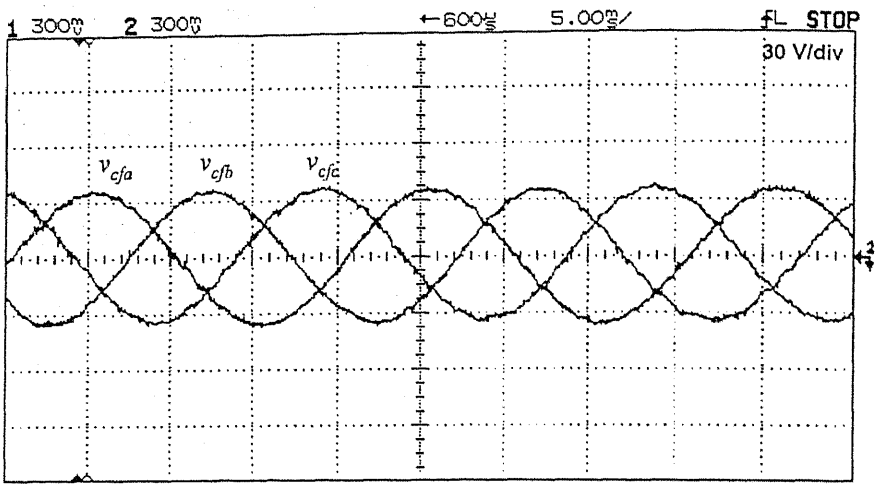


Fig. 6.21 Three-phase voltage waveforms of capacitors before connecting DSTATCOM to the PCC

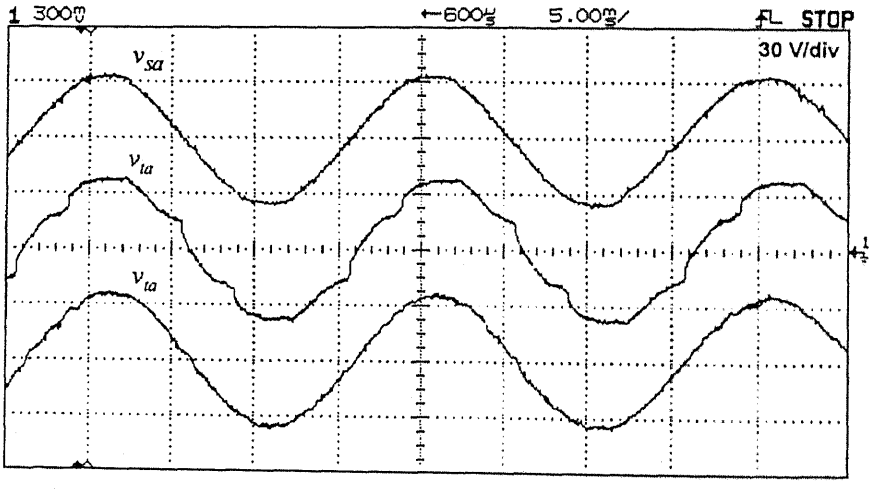


Fig. 6.22 The source voltage, terminal voltage (before and after DSTATCOM connection to the PCC)

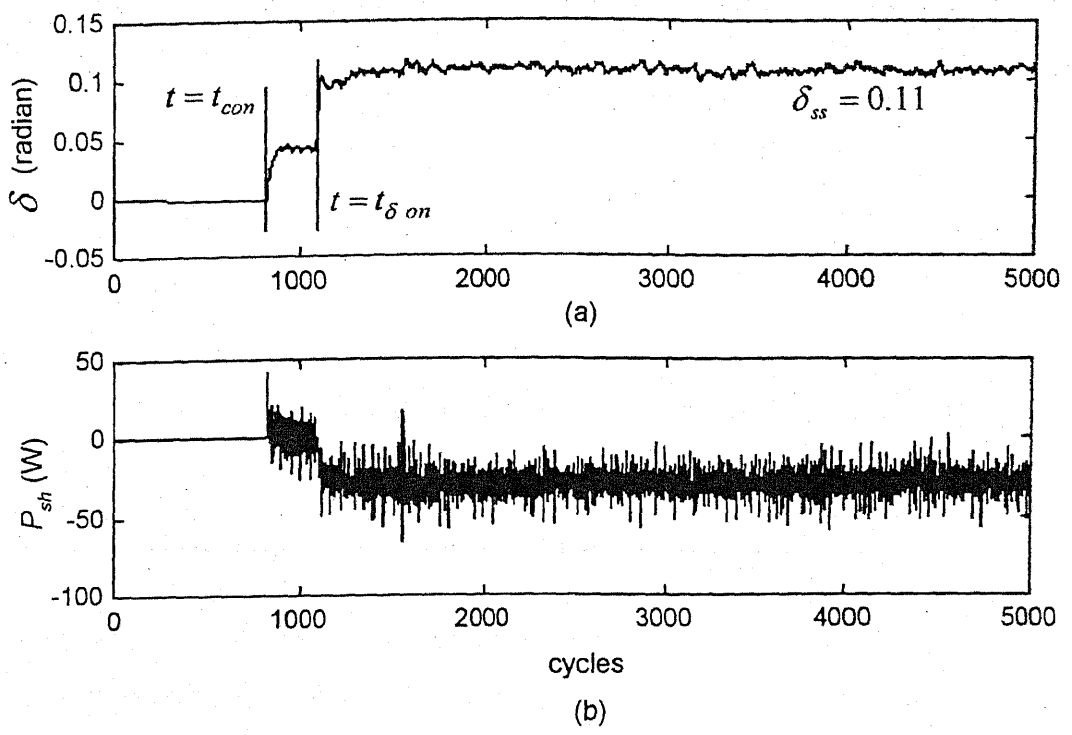


Fig. 6.23 (a) Variation of δ (b) Variation of P_{sh} (c) Variation of v_c for harmonic load only

6.4.3 Unbalanced and Non-linear Load

The load contains:

- Three-phase unbalanced R-L load $R_a = 40\ \Omega$, $R_b = 50\ \Omega$, $Z_c = 72 + j\ 84\ \Omega$
- Three-phase diode full bridge rectifier drawing a dc current of 0.5 A

Before voltage regulation, terminal voltage is distorted as shown in Fig. 6.24. The regulated voltage is shown in Fig. 6.25. As seen from the figure that in steady state δ settles around 10°. The variation of δ and average shunt power in shunt link are shown in Fig. 6.26 (a) and (b) respectively.

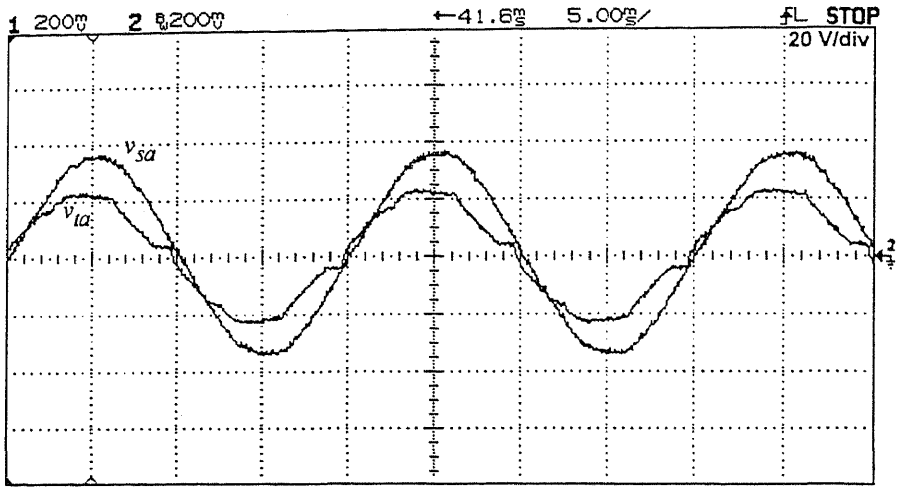


Fig. 6.24 The source and terminal voltage in phase-*a* without voltage regulation

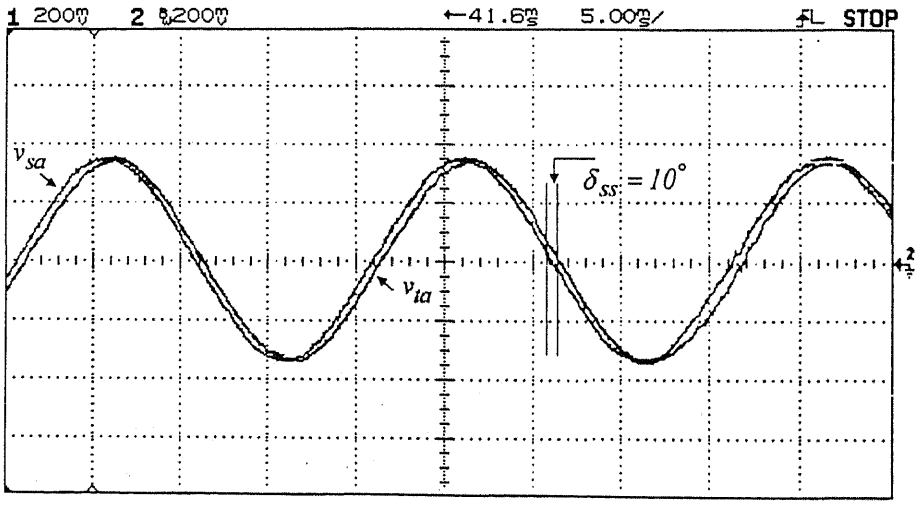


Fig. 6.25 The source and terminal voltage in phase-*a* with voltage regulation

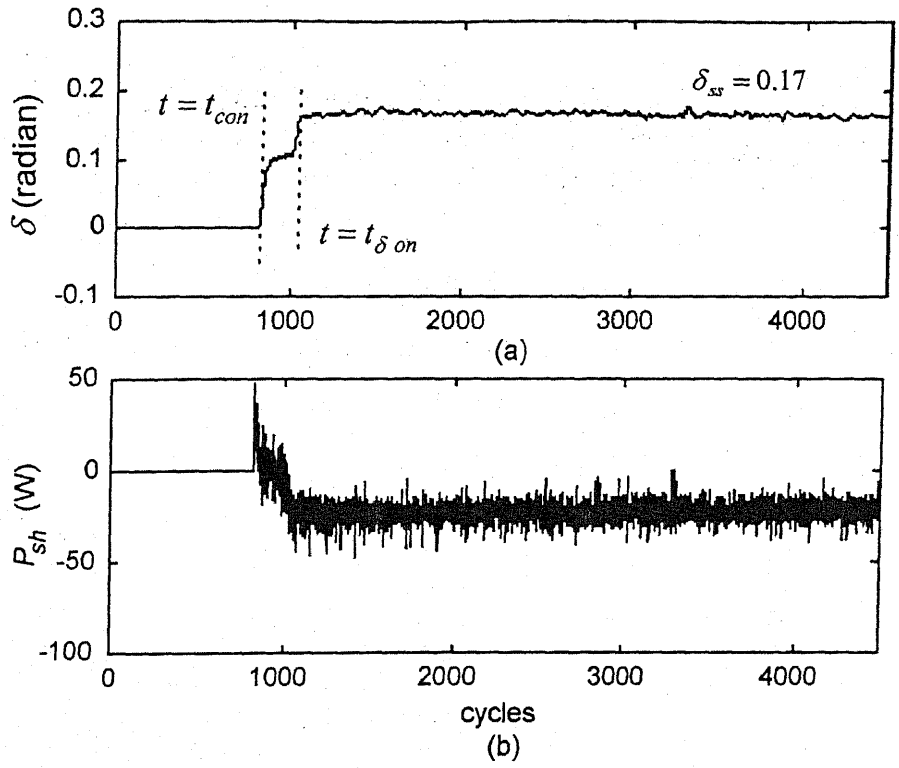


Fig. 6.26 (a) Variation of δ (b) Variation of P_{sh} for unbalanced load

6.4.4 Transient Performance of Voltage Regulator

The load in phase-*a* is changed by switching off the passive load suddenly and retaining only rectifier load. Again after approximately one and half cycle, the load is switched back to normal. The load current and terminal voltage in phase-*a* are shown in Fig. 6.27. It is seen from the voltage waveform that the terminal voltage is not affected by change in the load. Thus the voltage regulator is able to regulate the voltage at the bus under transient load.

In the next test, the outer voltage loop of Fig. 6.4 and P_{shref} is arbitrarily set to zero initially, followed by two step changes to +20 and –20 W. The results are shown in 6.28. The balanced resistive load of 50 Ω in each phase is considered. The source voltages are nearly balanced and sinusoidal with a value of 36 V peak. The terminal voltage is also regulated at 36 V peak. For $P_{shref} = 0$, this δ settles at 0.052 radian. Later on, at 1000^{th} cycle, P_{shref} is made +20 W, which means that the inverter now supplies to 20 W power to

the terminal bus, therefore P_{sh} is also 20 W. Thus, the source is relieved of supplying some of the real power required by the load. Hence δ decreases to 0.0082 radian. It takes about 35-40 cycles to settle down. At 3000th cycle P_{shref} is made -20 W and P_{sh} is tracking around -20 W. Now source is supplying 20 W to the inverter in addition to supply to the load power. Therefore δ increases and settles at 0.11 radian.

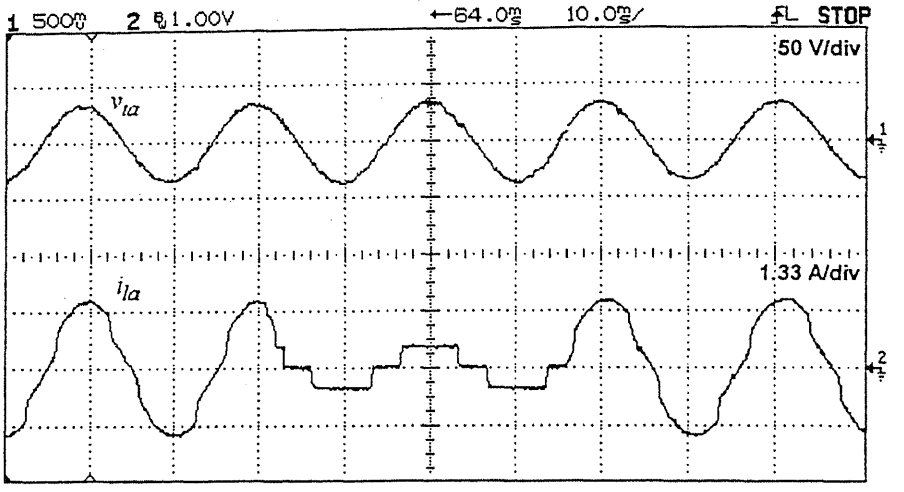


Fig. 6.27 The terminal bus voltage under load changing conditions

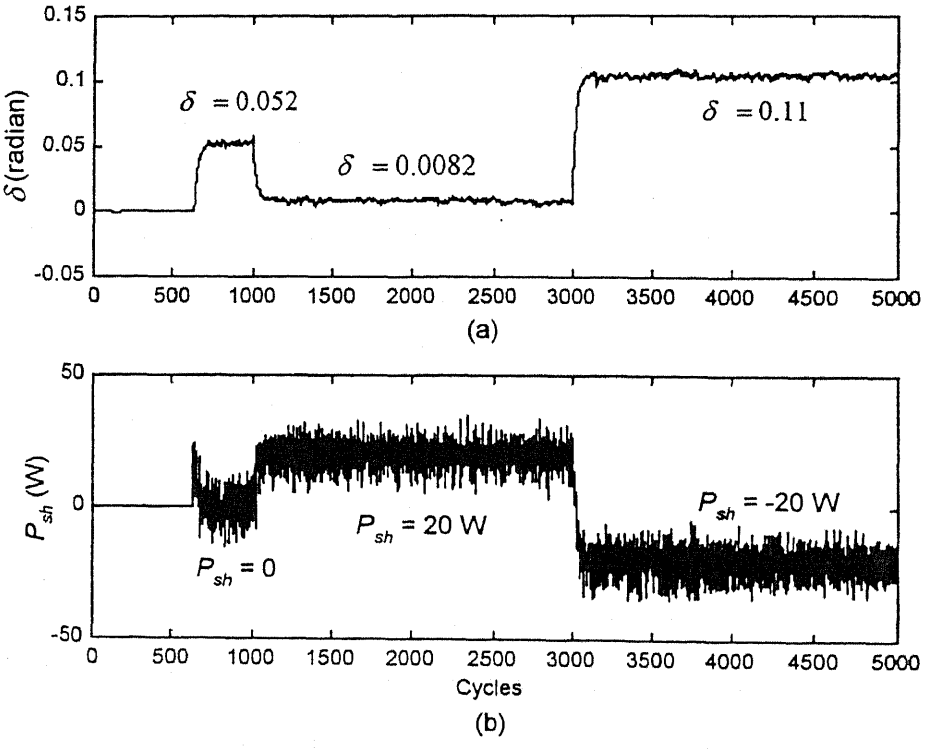


Fig. 6.28 Transient performance of δ control loop (a) δ variation (b) P_{sh} variation

6.4.5 Terminal Voltage Regulation in Under and Over Voltage Conditions

The source voltage is increased to 40 V from the nominal 36 V. The voltage waveforms of source and terminal are shown in Fig. 6.29. The variation of δ and P_{sh} are shown in Fig. 6.30. In the steady state, δ settles at 0.118 radian (6.76°). Further, the source voltage is decreased to 32 V peak. The voltage waveforms of source and terminal voltage are shown in Fig. 6.31, while variation of δ is shown in Fig. 6.32. Since the source voltage is less than the nominal voltage, its steady state value is 0.178 radian, which is larger than the previous case, where source voltage was above the nominal value.

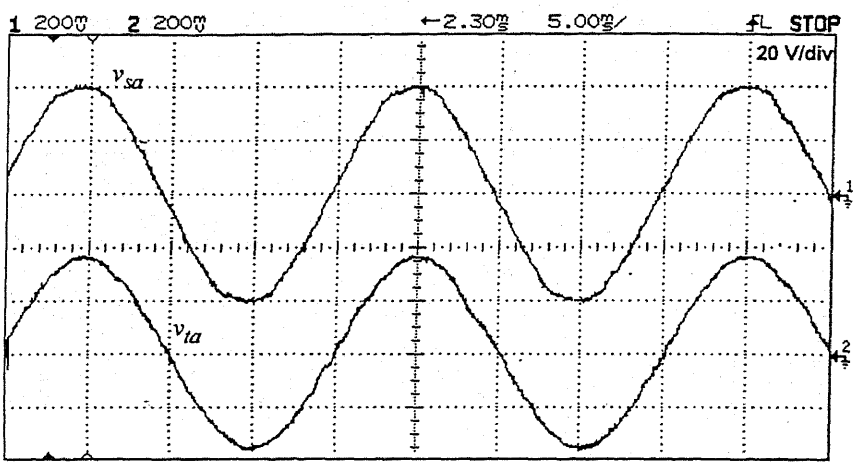


Fig. 6.29 Source voltage and PCC voltage in phase-*a*

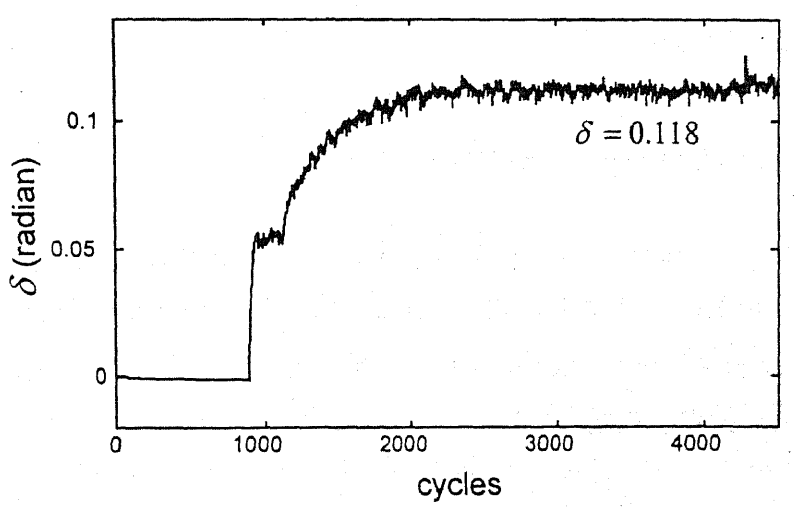


Fig. 6.30 Variation of δ when source voltage is more than nominal value

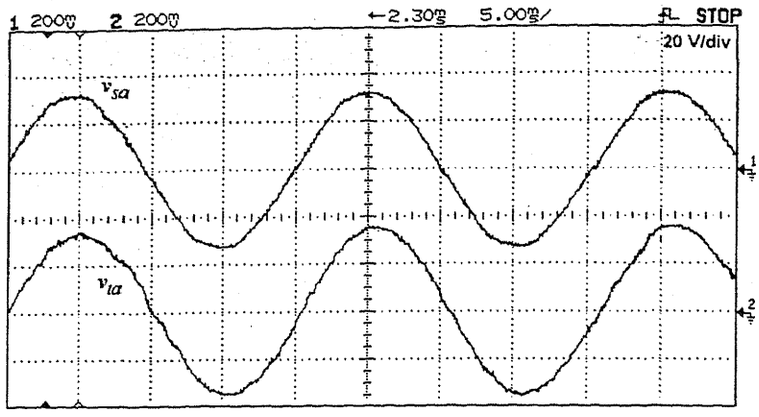


Fig. 6.31 Source voltage and PCC voltage in phase-*a*

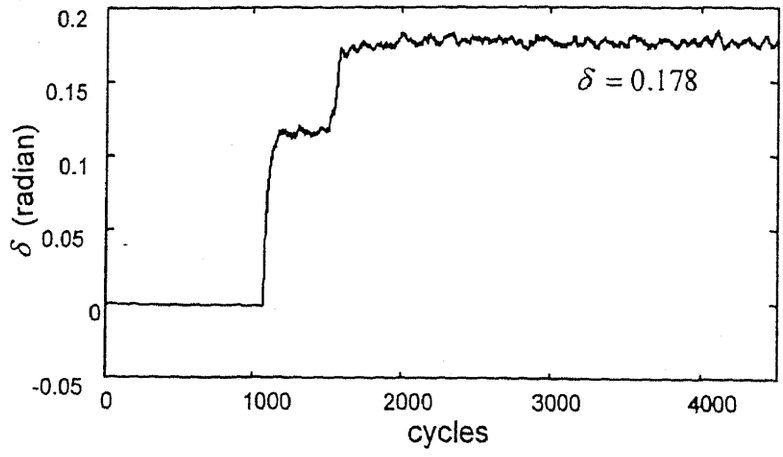


Fig. 6.32 Variation of δ when source voltage is less than nominal value

6.4.6 Unbalanced Source Voltages

The source voltage in phases *a* and *c* is 32 V peak, while as in phase *b* voltage is 40 V peak. These are shown in Fig. 6.33. After voltage regulation, the terminal voltage is regulated to 36 V peak in each phase. In the steady state, δ settles at 0.14 radian. The regulated terminal voltages are shown in Fig. 6.34.

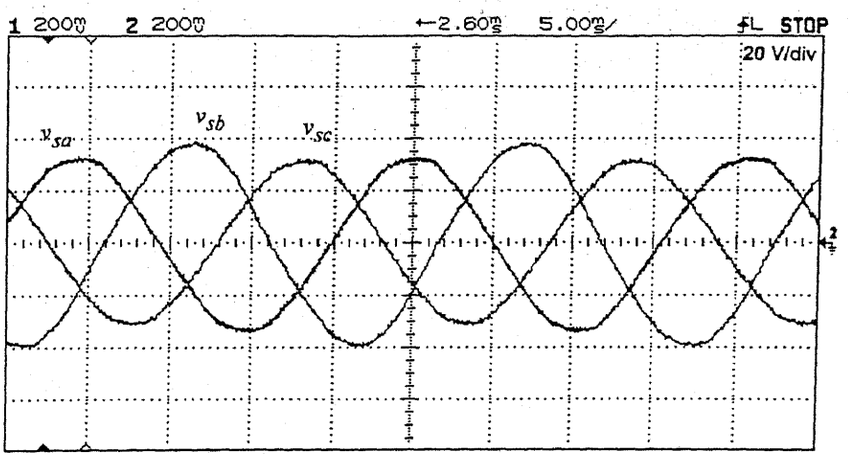


Fig. 6.33 Unbalanced sources voltages

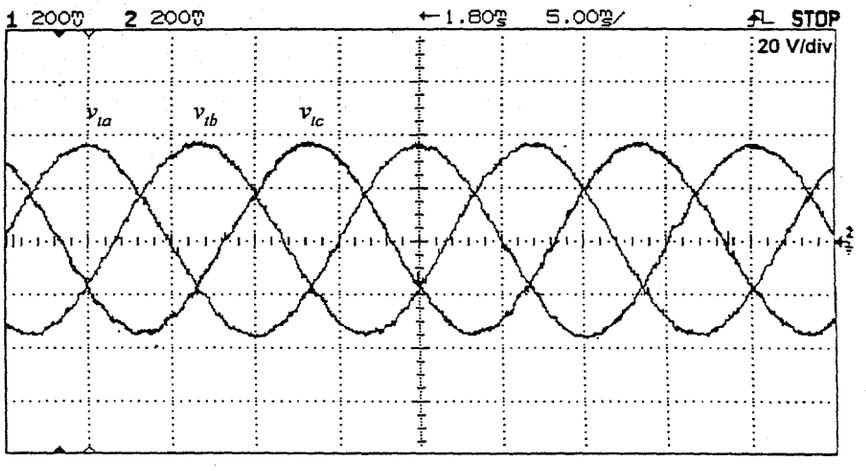


Fig. 6.34 Balanced terminal voltages after voltage regulation

6.5 CONCLUSIONS

In this chapter, a deadbeat control algorithm is proposed to regulate the voltage of the terminal bus at nominal value. The closed loop dc capacitor voltage control is described and implemented. The various cases of load configuration i.e. unbalanced R-L, pure harmonic load, and their combination are considered to demonstrate effectiveness of the algorithm. The transient in load is also considered. The algorithm is also shown to work in over voltages, under voltages and unbalanced source voltages conditions. The detailed

simulation and experimental results are presented. The results indicate that the algorithm is capable of holding the bus voltage at PCC to specified value in the presence of various source side and load side disturbances.

CHAPTER 7

CONCLUSIONS

The general conclusions drawn from the thesis and some suggested new directions are presented in this chapter.

7.1 GENERAL CONCLUSIONS

The general conclusions of the thesis are summarized below.

1. A shunt algorithm based on generalized instantaneous reactive power theory has been proposed and applied to various kinds of compensation schemes. The expressions for compensator reference currents are very general and true for balanced and unbalanced voltages and loads, with or without zero sequence components. Simulation and experimental results confirm that the shunt algorithm is computationally efficient.
2. The proposed algorithm has been extended for unbalanced source voltage operation by introducing a fictitious set of system voltages, which gives the same average load power. The modified filter current algorithm gives correct compensation to obtain any desired source power factor for unbalance in source voltage magnitudes and/or phase angles. This is termed as Equal Current Strategy as the compensated 3-phase source currents are balanced sinusoids. For the special case of unity power factor operation, an alternative Equal Resistance Algorithm has also been obtained.
3. Various topologies of shunt active power filters are studied. Their merits and demerits are discussed. It is found that neutral clamped inverter topology is suitable for independent tracking of three-phase reference currents. But if the zero sequence currents in neutral path contains dc component the voltage of the two capacitors become unbalanced. This topology is chosen for ac load compensation for balanced

and unbalanced source voltages using with proposed algorithms. A closed loop control of dc capacitor voltage is described.

4. To compensate dc loads, a new DSTATCOM topology called inverter-chopper topology is proposed. It consists of two dc storage capacitors and a three-phase voltage source inverter, is proposed for three-phase, four-wire distribution systems and a chopper circuit. A detailed state space model of the compensator is derived. The problem of voltage imbalance in case of loads containing dc component in line currents is discussed in detail. It has been shown that voltage imbalance in capacitors results in degraded performance of the compensator. To ensure the correct performance of the compensator, the voltage of the capacitors should be regulated to the reference value.

   A two-quadrant chopper circuit of the compensator is employed to regulate the voltage of the capacitors. The six different control schemes of chopper control are discussed. It has been shown that the control schemes are able to stabilize the voltages of the capacitors close to the reference value. This ensures the correct performance of the compensator.

5. If the load is supplied by a feeder, i.e., the source is non-stiff, straightforward application of compensation algorithms will result in unacceptable distortions in source currents and PCC voltage.

   The following measures are taken to eliminate distortions due to the inverter switching:

   - A shunt capacitor is connected across the PCC.
   - Fundamental of the PCC voltage is extracted.
   - A state feedback control is employed.

   The reference for state feedback controller are fundamental PCC voltage, fundamental capacitor current and injected shunt current generated from the compensator algorithm. The state feedback control of inverter with shunt algorithm gives the best performance even under unbalanced source voltages. In this control,

the ac filter capacitor is used in a control loop. Most importantly, the switching frequency components are not directly seen in terminal voltage and source currents.

6. A DSTATCOM in voltage control mode is shown to regulate the bus voltage at the nominal value for unbalanced and distortions in both supply voltage and load currents. The DSTATCOM works under deadbeat control rather than full state feedback control. The magnitude of the PCC bus voltage can be arbitrarily chosen, while its phase angle is controlled through outer dc capacitor voltage loop and inner shunt power loop. A deadbeat control algorithm is used to operate DSTATCOM in voltage control mode.

   The various cases of load configuration i.e. unbalanced R-L, pure harmonic load, and their combination are considered to demonstrate effectiveness of the algorithm. The transient in load is also considered. Over-voltage, under-voltage and unbalance in source voltage are also considered to demonstrate the effectiveness of the algorithm.

7.2 SCOPE FOR FUTURE WORK

Some suggestions for future work are:

1. A digital signal processing (DSP) dedicated system may be used for implementation of the shunt compensation schemes. Use of DSP system avoids the interrupt clash problems in PC.
2. A menu driven program may be developed in C/C++ for all schemes of compensation presented in the thesis.
3. Multi-level inverter can be used for further improvements in shaping of compensator currents that may result in reduction of switching frequency harmonics.

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APPENDIX A

EXPERIMENTAL SET-UP

In this appendix an experimental set-up has been described for the verification of the proposed theories of shunt compensation for balanced and unbalanced, stiff and non-stiff source voltages. The experimental results presented in chapters 2-6 in detail have been obtained using this set-up. The hardware set-up requires various control cards, power circuit, drive circuit of the inverter and PC interface. These components of hardware set-up have been described in detail. The discussion covers the details of various control cards and the power circuit.

A.1 POWER CIRCUITS

The power circuit of the experimental set-up is shown in Fig. A.1. The main power circuit consists of the three-phase, four-wire variable voltage source, three-phase load, voltage source IGBT inverter and chopper. The inverter dc bus is connected to an auxiliary supply, which consists of a single-phase transformer and diode rectifier circuit for pre-charging the dc storage capacitors. The three-phase inverter output is connected to the point of common coupling (PCC) through interface inductors.

The prototype for experimental verification is at rather moderate voltage, so a three-phase variac of rating 270 V and 15 A, has been used. This provides a balanced variable voltage source at desired voltage level for experimentation. To obtain unbalance in source voltage magnitudes and phase angles, single-phase autotransformers and a phase shifter have been used. The inductance of a three-phase variac adds to the impedance of the ac. However the supply can be considered to be a stiff source for all practical purposes. In the experiments requiring non-stiff voltage source extra impedance in each phase, has been added to model the feeder impedance. The control circuits require feedback of various voltage and currents at different points in the power circuit. For this purpose Hall effect voltage and current transducers have been used. These are shown as HV1-HV6 and HC1-HC12 for voltage and current transducers respectively in Fig. A.1.

Three-phase Load: Three-phase load consists of three unequal impedances and three-phase diode rectifier that can be operated in either full bridge (6 pulse) or half bridge (3 pulse) mode. The full and half bridge mode is selectable by a switch. Thus this load configuration is able to provide (i) Unbalanced sinusoidal load currents (ii) Unbalanced non-sinusoidal load currents and ac neutral currents (iii) Unbalanced non-sinusoidal load currents with ac and dc component in the neutral current. Hall effect voltage transducers HV1-HV3 and current transducers HC1-HC3 are employed to measure the voltages at the PCC and load currents respectively. The current transducers HC4 and HC5 are used to sense the neutral currents in the direction shown in Fig. A.1.

Three-phase Inverter: The voltage source inverter (VSI) in a current control mode is intended to inject the harmonic currents at point of common coupling (PCC) so that it results in the desired compensated source currents. The voltage source inverter is comprises of six IGBT switches S_1-S_6, each with anti-parallel diode and two dc storage capacitors C_1 and C_2. The IGBT inverter consist of top switches S_1, S_3, S_5 and the bottom switches S_4, S_6, S_2. From the middle of top and bottom switches in each leg of the inverter, the interface inductors R_f-L_f are connected to the PCC. The IGBT inverter is controlled in a hysteresis band current control mode. The current transducers HC6-HC8 are used to measure the compensator currents, which are fed back to the inverter control circuit.

Pre-charging Circuit: An auxiliary supply is obtained using a single-phase transformer and diode rectifier. The auxiliary supply is needed to pre-charge the dc capacitors C_1 and C_2 to the desired voltage level. In normal operation of the inverter, the main switch MS-1 in Fig A.1 is open, which disconnects the auxiliary power supply to the capacitors. The total capacitor voltage is then maintained by drawing some real power from the source in a balanced manner.

DC Chopper Circuit: When the load currents contain the dc components the dc capacitors may become unbalanced if the neutral current also contains the dc component. To remove this unbalance, an additional two-quadrant chopper circuit is used (Fig. A.1). The chopper circuit consists of two IGBT switches S_7 and S_8 each with anti-parallel diodes and chopper inductor R_{ch}-L_{ch}. The chopper switches are controlled using different control schemes to obtain the balance in dc capacitor voltages. Voltage transducers HV4-HV6

measure the voltages across dc capacitors C_1, C_2 and total capacitor voltage. The current transducer HC9 measures the chopper current. These signals are used as feedback to the chopper control circuits.

Non-stiff Source: In case of non-stiff supply voltage source, PCC voltages are distorted due to switching action of PWM inverter. This may lead to an erroneous compensation as the compensation algorithm assumes the balanced supply voltages. To overcome this the ac capacitors (C_f) between load neutral n and PCC are employed to remove the distortions in PCC voltages. The additional voltage transducers HV7-HV9 and current transducers HC13-HC15 are employed to measure the ac capacitor currents. One more voltage transducer HV10 is needed to provide the master clock for the synchronization of terminal voltages and source voltages. A state feedback controller is employed to regulate the terminal voltages, which uses the signals from above transducers.

A.2 BLOCK DIAGRAM OF OVER ALL CONTROL SYSTEM

The block diagram for PC interfacing and other controllers is shown in Fig. A.2. The low voltage signals from the Hall effect transducers connected in the power circuit (Fig. A.1) are used as inputs to various controllers. In the Fig. A.2, the load current signals are obtained from Hall effect current transducers HC1-HC3 and the terminal voltages are obtained from Hall effect voltage transducers HV1-HV3. The total dc capacitor is sensed using HV6. For chopper control the dc capacitor voltages v_{c1} and v_{c2} are sensed through HV4 and HV5, while the chopper inductor current is sensed through HC9. For nonstiff source the inverter filter currents, ac filter capacitor voltages and currents are obtained using HC6-HC8, HV7-HV9, HC13-HC15 respectively. For synchronization a clock is derived from phase a source voltage using HV10.

An IBM compatible P-II. PC acquires above mentioned signals through ADC channels of a data acquisition card PCI 9118DG, whose details are given in the APPENDIX B. Based on these quantities, the programs for shunt algorithms for various types of compensation, e.g. reference current tracking, state feedback control, chopper control for dc capacitor voltage balance etc, written in C/C++, are run. For reference current tracking the

computation generates these instantaneous reference quantities for compensator. These reference currents are converted to analog values through three DACs.

The actual compensator quantities are obtained using Hall effect voltage and current transducers. On the basis of these reference and actual quantities, PWM controller and blaking circuit for each phase is used to generate the logic outputs of the PWM control circuit which are then given to the gate drive circuit of the IGBTs. For state feedback control and voltage controlled DSTATCOM, the switch states are directly computed in the PC and sent to the gate drive circuits. The DC power supply provides different dc voltage levels to the PWM control circuit. The gate drive circuits of the IGBT switches are supplied through the isolated power supplies.

In the following sections the different components of the block diagram shown in Fig. A.2 are described in detail.

A.3 PWM CONTROLLER

The purpose of the circuit is to modulate the compensator current in PWM VSI. There are four such control cards each for one phase and one is for chopper current control in hysteresis band. Theses are shown in Fig. A.3. The reference current, i_f^* generated by shunt algorithm is modulated by positive and negative band, i.e. $i_f^* \pm h$ using OP AMPs TLO081 at the initial stage of the circuit. The modulated reference current signal is then compared against the actual compensator current i_f using comparator LM 311. If $i_f > i_f^* + h$ (which also implies $i_f > i_f^* - h$) the outputs of both the comparators are logic 1 (+5 V) making binary states of the comparators Y_1Y_2=11. Similarly, if $i_f < i_f^* - h$, (which also implies $i_f < i_f^* + h$), Y_1Y_2=00. For any other value of i_f between $i_f^* - h$ and $i_f^* + h$, Y_1Y_2=01. The states Y_1Y_2=11 is decoded using NAND gate making $\overline{R} = 0$, $\overline{S} = 1$, which resets the latch and therefore $Q = 0$, $\overline{Q} = 1$. Similarly the output comparator states Y_1Y_2=00 is decoded making $Q = 1$, $\overline{Q} = 0$. If Y_1Y_2=01, the inputs to the latch are inactive, $\overline{R} = 1$, $\overline{S} = 1$ and the latch retains previous states.

The Hall effect current transducers HC6-HC8 in Fig. A.1 are used for measurement of actual compensator currents. Running shunt algorithm on IBM compatible PC generates the compensator reference currents.

The outputs of the latch Q and $\overline{Q}$ are not directly fed to the gate driver to the IGBTs. During the state transition if both the states are on it will result in shorting of the dc supply, commonly known as 'shoot through fault'. A blanking circuit is employed to remove this problem. The circuit is designed using monostable 74LS123 and AND gate 7408. The blanking circuit ensures that outgoing switch is turned off first, and only then incoming switch in the same leg is turned on. This circuit is described in detail in the next Section.

This logic operation ensures the proper gating of the IGBT switches through driver circuit, which enables VSI to track the actual compensator currents within lower and upper limits of the reference currents.

A.4 BLANKING CIRCUIT

The purpose of blanking circuit is to provide protection to IGBTs of the inverter so that the IGBTs in the same leg do not remain on simultaneously. This is very important protection to the IGBTs. In the heart of the blanking circuit is dual mono the mono shot generator IC chip 74LS123N whose pin out is shown in A.4. Both of these units have been used to generate short pulses, $\overline{Q}_{1\,shot}$ and $\overline{Q}_{2\,shot}$. The width of the shot pulse is controlled by RC network connections as shown in Fig. A.4 (b) is given by,

$$t_d = 0.45\, R_{ext} C_{ext}$$

For R_{ext}=120 KΩ and C_{ext}=100 nF the value of t_d is 5.4 μs.

The timing diagram has been shown in Fig. A.5. The logic signal Q and its complimentary $\overline{Q}$ are ANDED with $\overline{Q}_{1\,shot}$ and $\overline{Q}_{2\,shot}$ respectively. The resulting waveforms G_1 and G_4 are shown in the Fig. A.5. It is seen in the figure that on time of the IGBTs switches in the same leg are delayed by time duration t_d with respect to the off time.

It ensures that there is a sufficient time delay between on and off transition for the IGBTs in the same leg. The experimental logical waveforms are shown in Fig. A.6. The time delay t_d in the figure is approximately 5.4 μs.

A.5 GATE DRIVE CIRCUIT OF IGBTs

A gate drive circuit with an overcurrent protection is shown in Fig. A.7. A gate drive circuit is designed on similar lines as given in [86]. The circuit incorporates the overcurrent feature. The protection scheme works on the concept that the drain source voltage of the IGBTs increases with the drain current for a given gate source voltage. The potentiometer P_2 is set such that the voltage at the variable point is one diode drop more than the drain source voltage corresponding to the peak value of the normal drain current. A RC circuit delays the activation of the protection circuit. As long as the drain current is within the normal limit, the drive signal is transmitted to the gate. When the drain current exceeds its limits the protection logic inhibits the drive signal from reaching the gate and a fault is indicated. The fault indication persists as long as the turn on process continues. The fault is also indicated in case of turn off failure.

A.6 CHOPPER CONTROL CIRCUIT

The chopper control circuit for open loop duty cycle control is shown in Fig. A.8. The heart of this circuit is a pulse width modulation IC chip SG3524. The circuit consists of few comparators and OP AMPs, logic gates and an IC chip SG 3524. In the above control only v_{c_2} and v_c are sensed. There is a separate PI controller that regulates the total capacitor voltage $v_c = v_{c_1} + v_{c_2}$ to a constant value $2V_{c\,ref}$. Thus v_c acts as a reference signal. To regulate one capacitor voltage (v_{c_2}) to a constant value $V_{c\,ref}$ means that another capacitor voltage (v_{c_1}) will automatically be regulated to the reference voltage. Thus there is only one feedback signal v_{c_2} which is regulated between limits $0.4v_c$ and $0.6v_c$. The two voltage signals are amplified by a factor of 4 using initial stage OP AMPs in Fig. A.7. At the next stage of OP AMPs the upper voltage 0.6 v_c and lower limit 0.4 v_c have been

created. v_{c_2} is now compared with these limits. If v_{c_2} is greater than 0.6 v_c, output v_{o1} from the comparator LM311 is logic 1 i.e. +5 V else the output is 0. Similarly, if v_{c_2} is less than 0.4 v_c, output v_{o2} from the comparator is logic 1 i.e. +5 V else the output is 0. If v_{c_2} is within these limits output from both comparators are 0, hence chopper action will be disabled. Thses outputs v_{o1} and v_{o2} are ANDED with PWM output from PWM IC chip SG 3254. The IC 3354 generates a PWM waveform whose duty cycle is decided by external signal. The Frequency of PWM output is set using C_T and R_T connected at 7 and 6 pin of SG 3254.

The circuit facilitates operation of one chopper switch at a time. The other switch is held open. When the polarity of dc component in load current changes, the switch which was off starts operating and the former becomes off. Thus, there is a transition in the states of the switches. The blanking circuit is employed to provides sufficient delay between on and off transition of chopper leg IGBT switches (S_7 and S_8). The logic signals are then passed through buffer CD4050 and are ANDED with over current pulse to protect IGBTs from over over current. Finally the processed signals are given to the base of the npn transistor CL100, whose collector is at +5 V. The outputs from transistors go to the driver circuit of the IGBTs. In the figure only one transistor whose output goes to gate driver of IGBT switch S_8. The another transistor's outpur goes to gate driver of IGBT switch S_7.

The chopper may also be controlled so that the chopper current is regulated within hysteresis band. The control circuit for this type of operation is identical to that shown in Fig. A.3 with the reference signal as i_{ch}^* and feedback signal i_{ch}. The outputs are connected to the chopper switches S_7 and S_8.

A.7 OVER CURRENT PROTECTION TO IGBTs

This circuit is employed for over current protection of rhe IGBTs in the inverter and chopper circuit shown in Fig. A.9. The minimum and maximum current limits ($I_{fa\max}$ and $I_{fa\min}$ for phase a) of compensator currents in each phase are used as one input of the comparators LM 311. The actual compensator currents (i_{fa} for phase a) for each phase is given as second input to both comparators. In Fig. A.9, the comparators of phase-a are only

shown. The set current limits represent the maximum positive and negative peak of filter currents against which the IGBTs are to be protected. If these current limits are violated the corresponding comparator gives output logic 1 (+5 V). This in consequence generates output logic 1 at the output pin of OR gate. There are similar circuits for phases *b* and *c*. The outputs from 3 OR gates (one for each phase) are acting as 3 inputs to 3 input OR gate CD 4075. Thus if the set currents limits are violated in any of the phase, the the output from 3 input OR gate is logic 1. If the currents limits in all 3 phases are within limit, the output from final OR gate is logic 0.

The output from 4075 is given to clock (pin 1) of JK flip flop 7476. The J input is held at +5 V and K input is at 0 V. On limit violation, the clock of flip flop is set to +5 V and therefore the output $\overline{Q}$ of the flip flop turns to be zero. This 0 logic signal is buffered using IC CD 4050. If $\overline{Q}$ becomoes 0 the LED glows and the stop signal is sent to each phase hysteresis band current controller card (Fig. A.3). This inhibits all gate signals to IGBTs. The circuit parameters are then checked and adjusted in a way as to achieve the filter current within limits and clear terminal of 7476 is touched to ground through push button to set $\overline{Q}$ to high hence bringing the inverter in active mode.

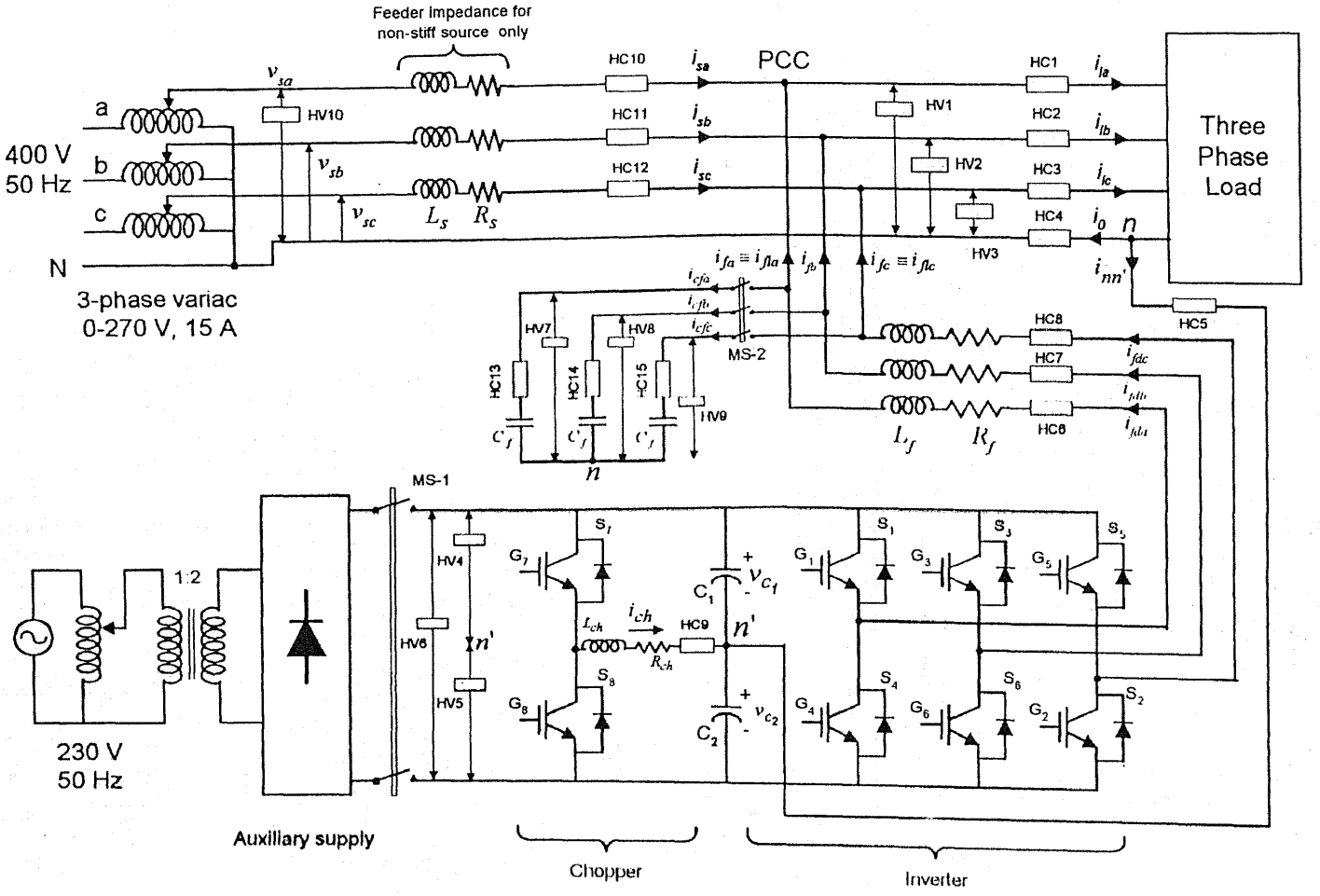


Fig. A.1 Power circuit for shunt compensator

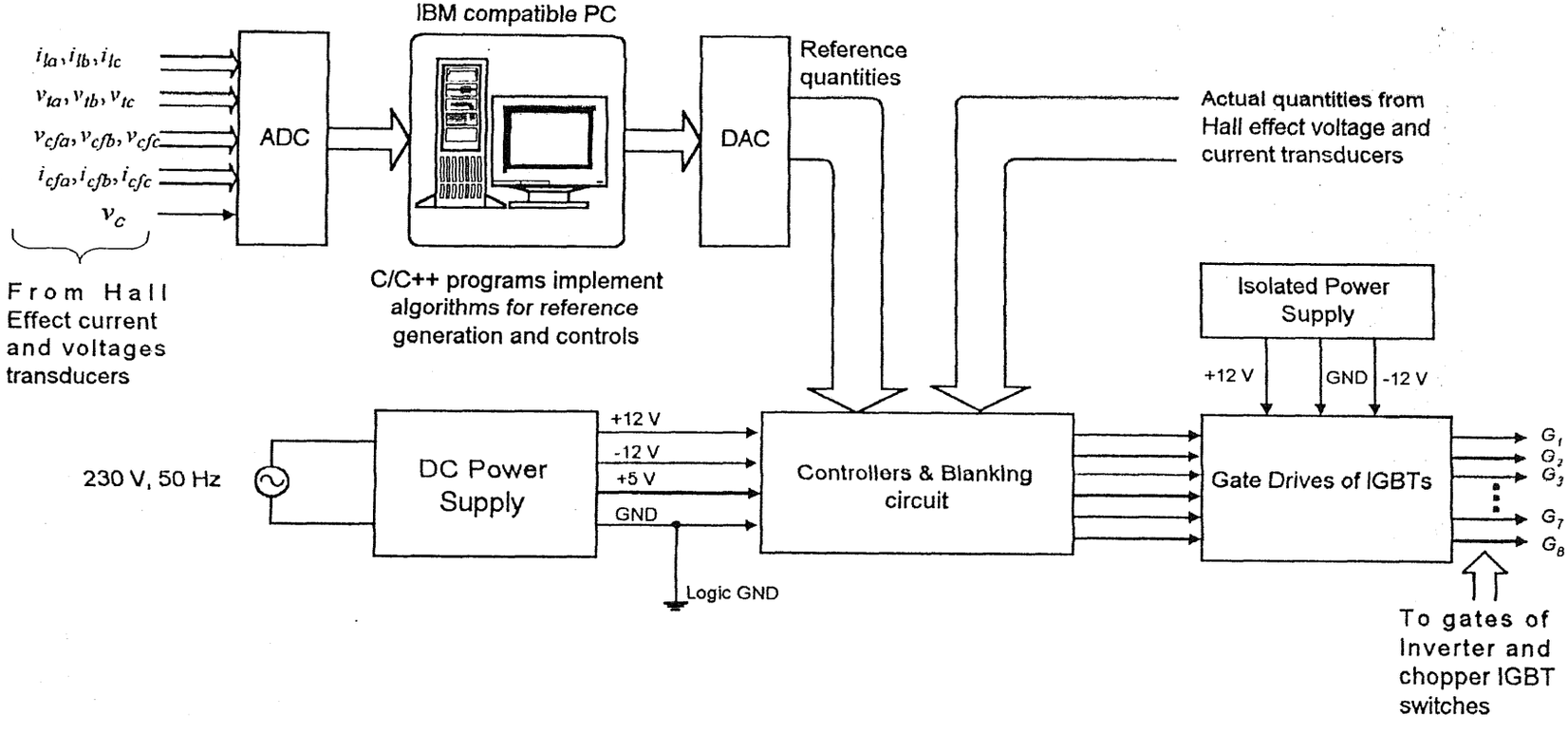


Fig. A.2 Block diagram of system and PC interface

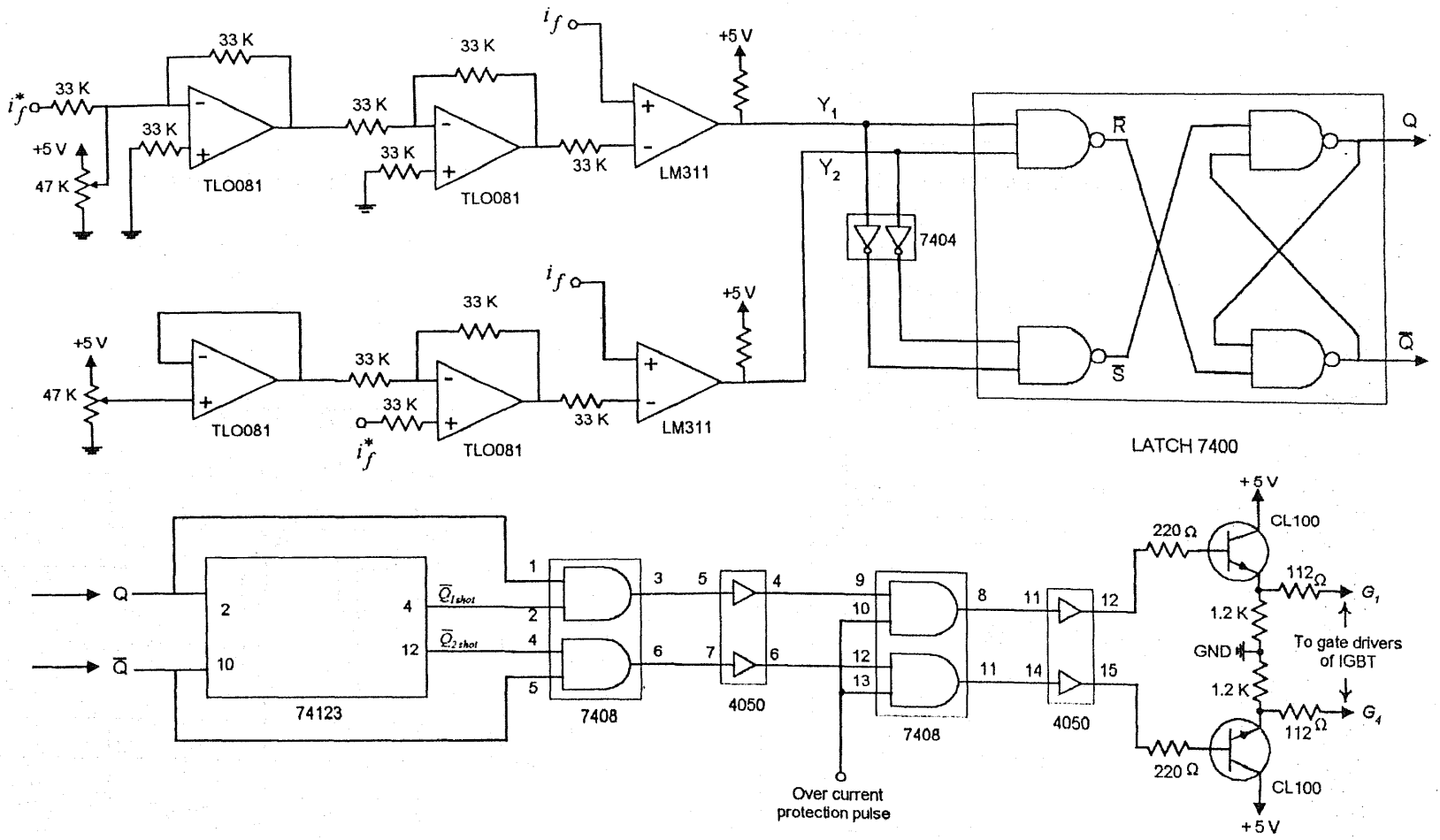
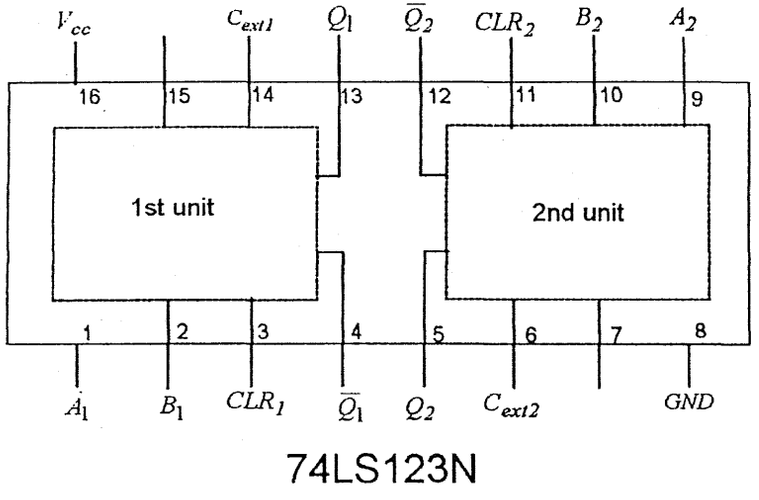
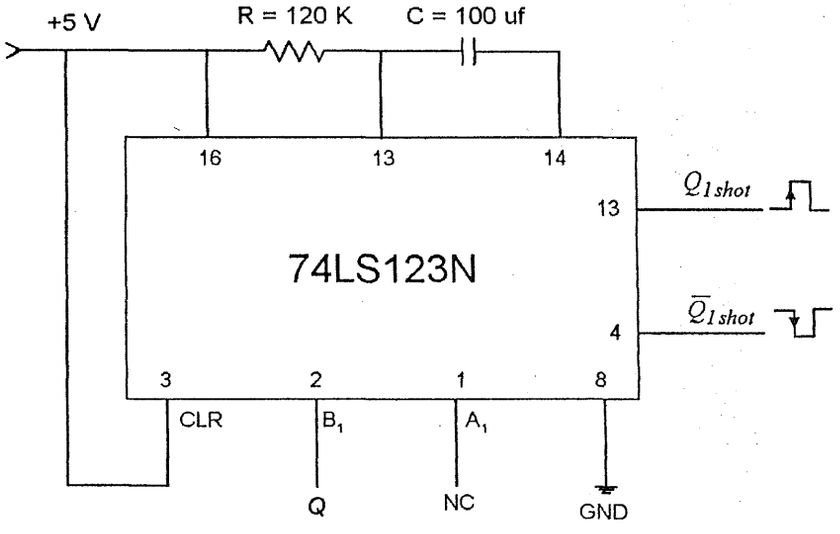


Fig. A.3 Current controller circuit of voltage source inverter



(a)



(b)

Fig. A.4 (a) Monostable 74LS123 (b) Blanking circuit to protect IGBTs from simultaneous ON state

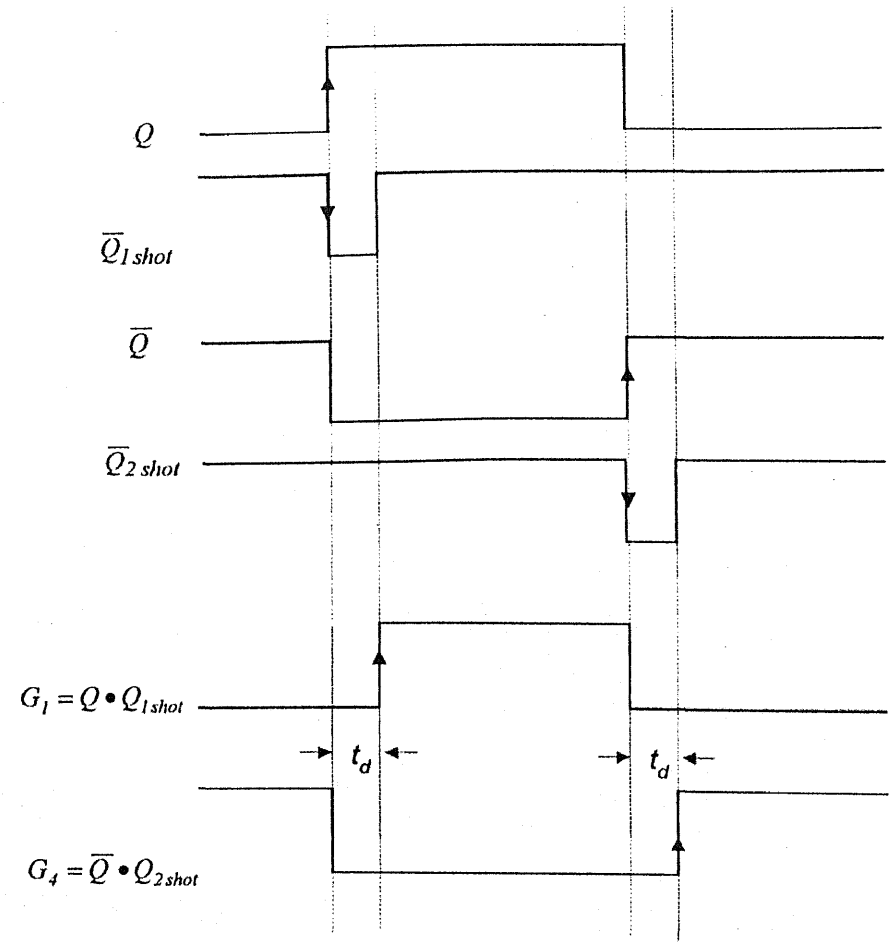


Fig. A.5 Timing diagram for gate signals of the IGBTs in the same leg

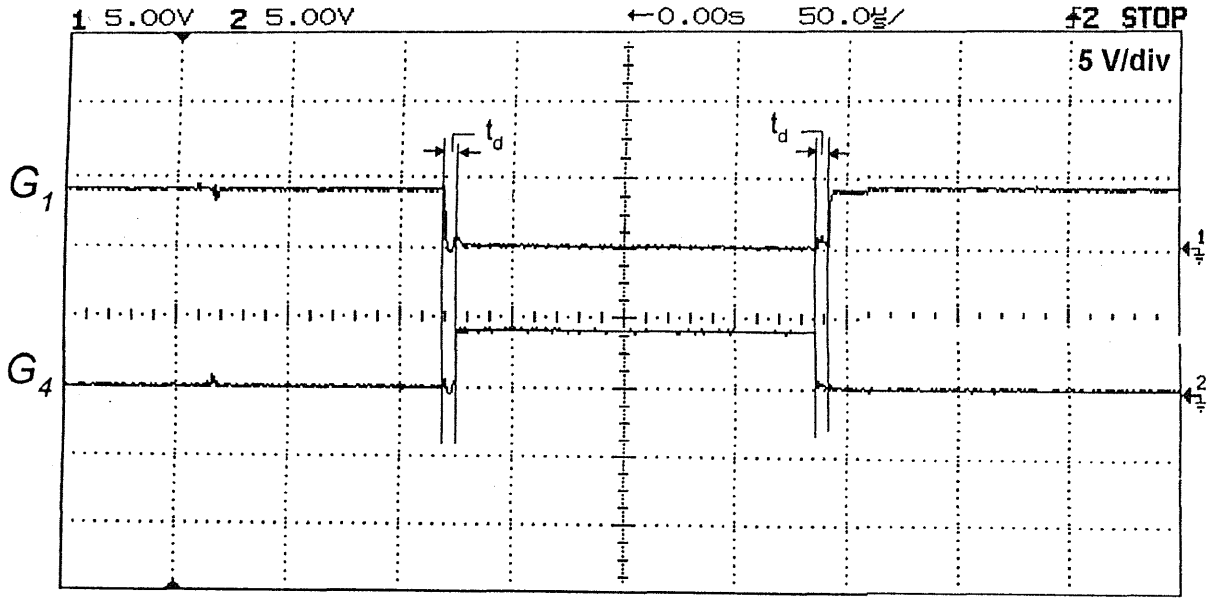


Fig. A.6 Timing diagram for gate signals of the IGBTs in the same leg: Experimental

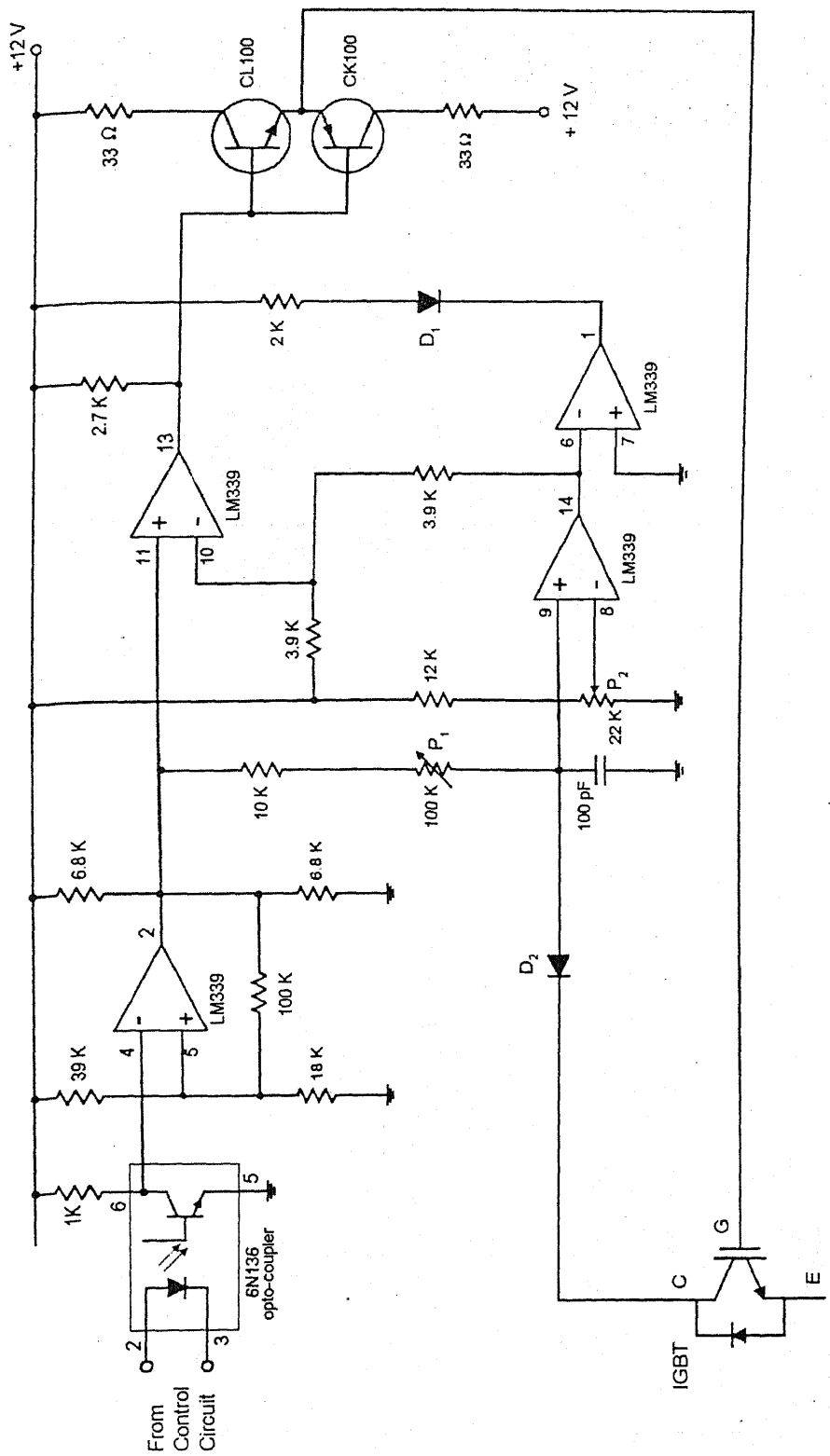


Fig. A.7 Gate drive circuit of IGBT

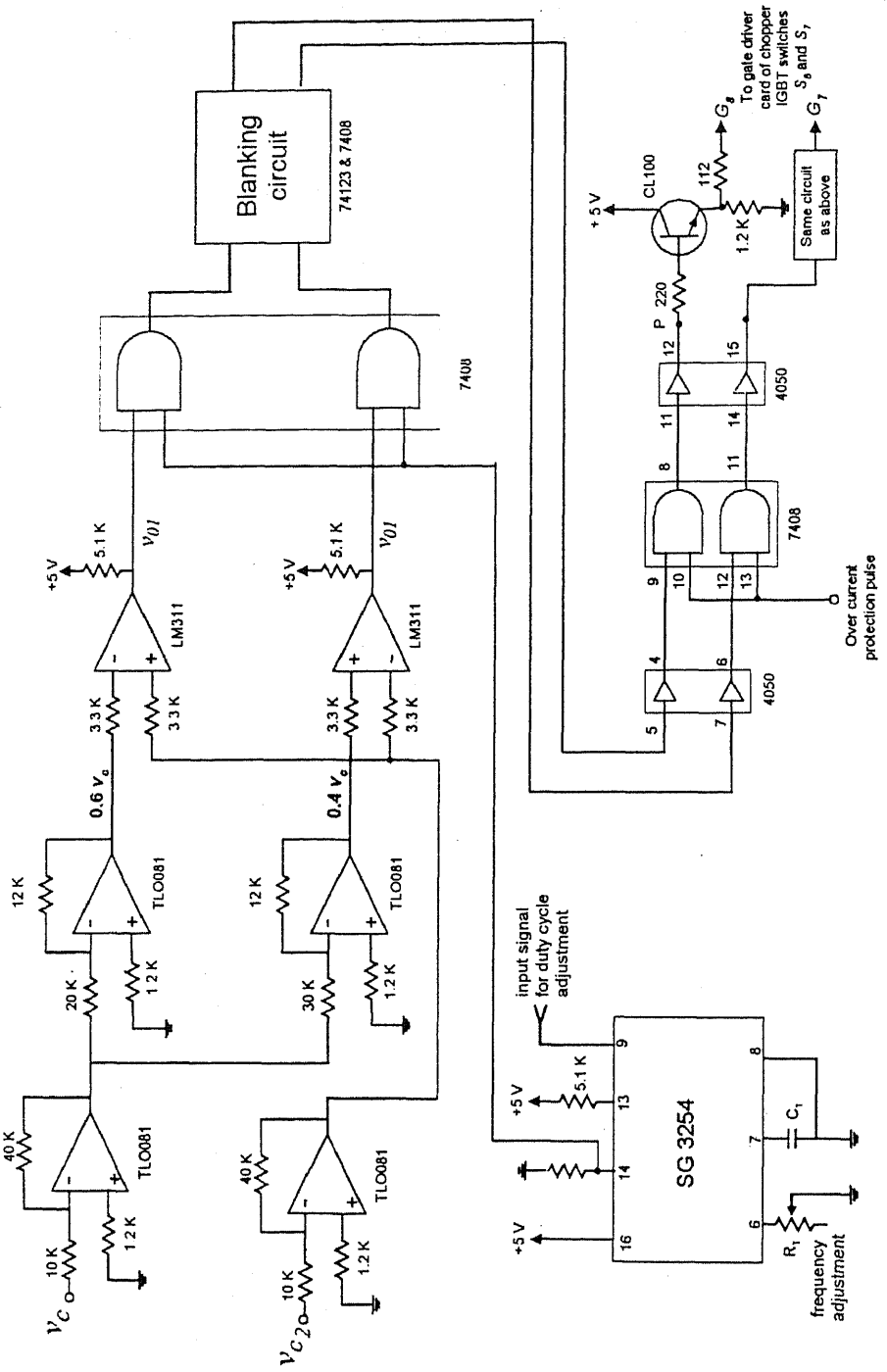


Fig. A.8 Chopper control circuit for open loop duty cycle control

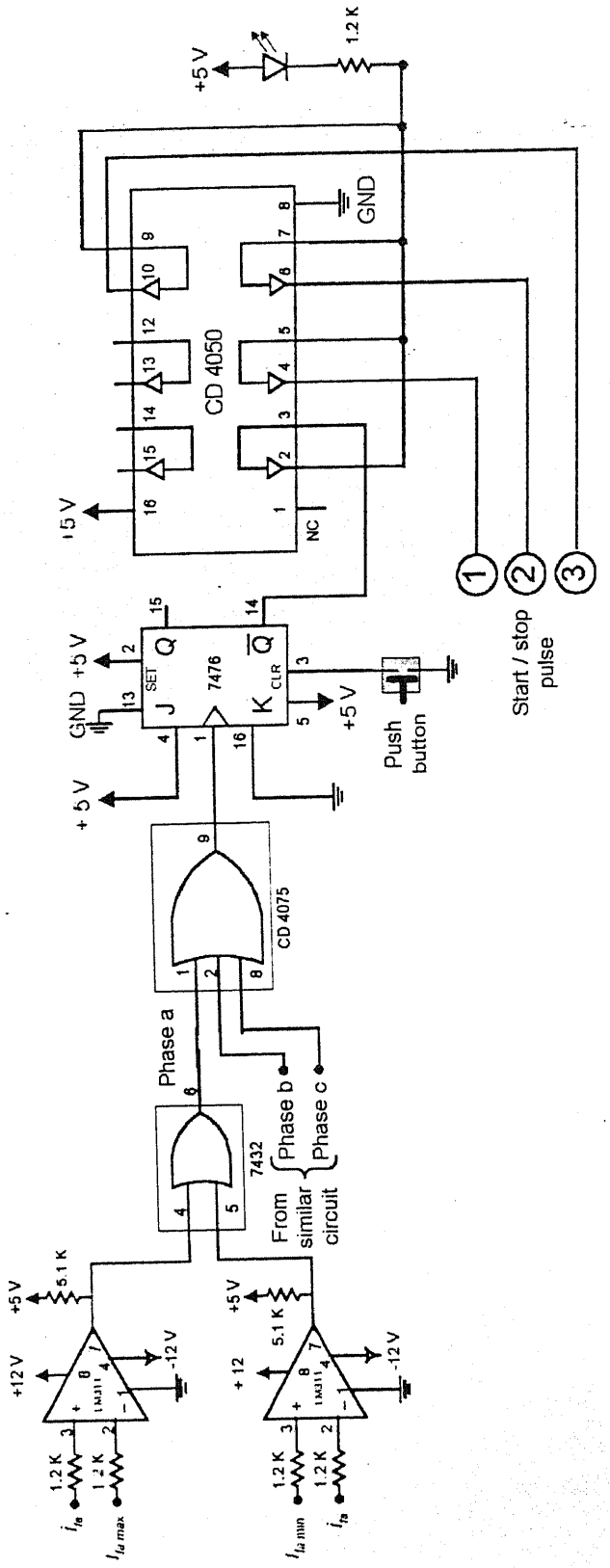


Fig. A.9 Over current protection circuit to IGBTs

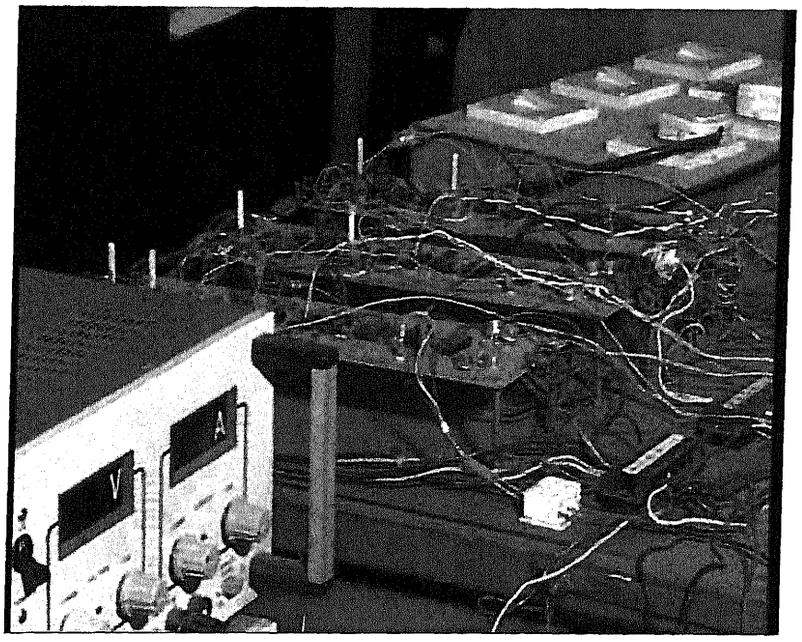


Fig. A.10 Photograph displaying hysteresis control cards

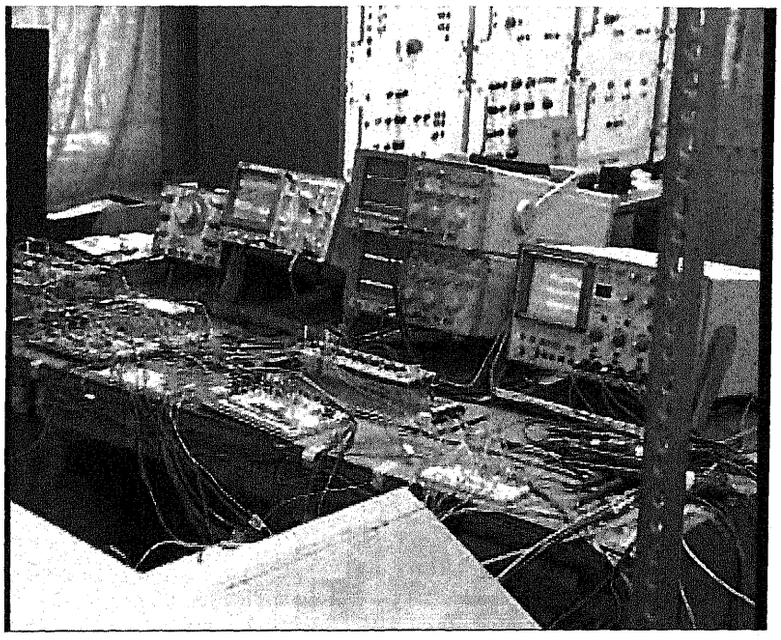


Fig. A.11 Photograph displaying various control circuits

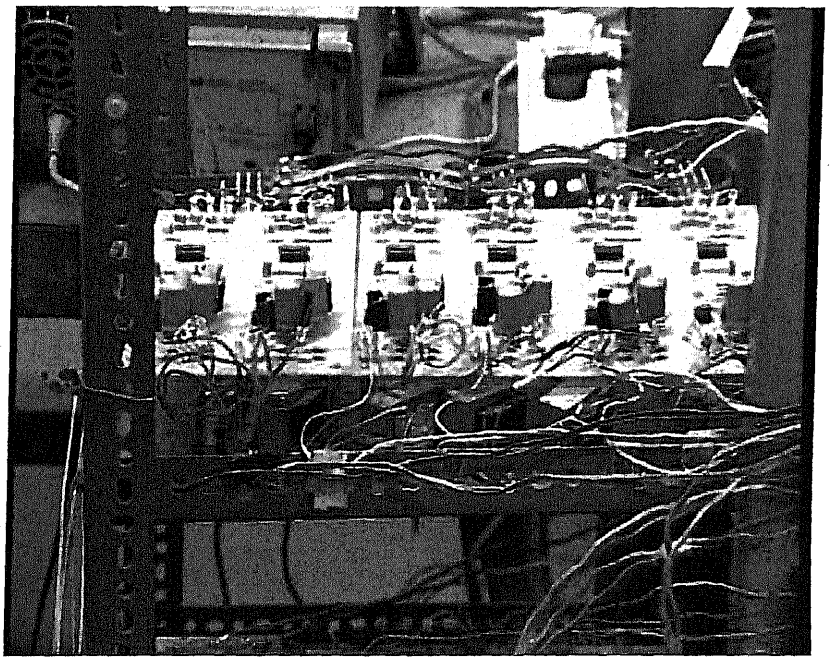


Fig. A.12 Photograph of gate drive circuit and the IGBTs

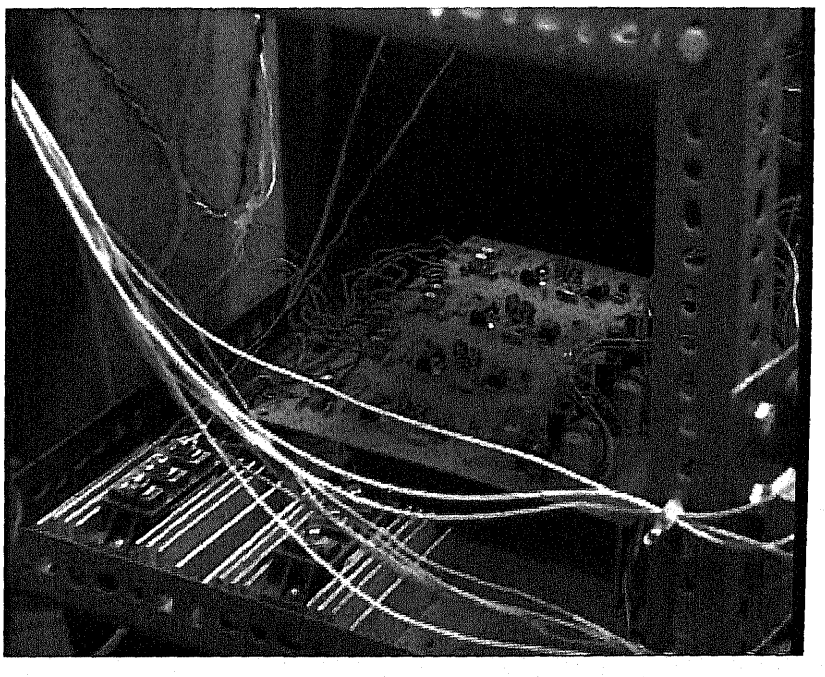


Fig. A.13 Photograph displaying IGBT modules

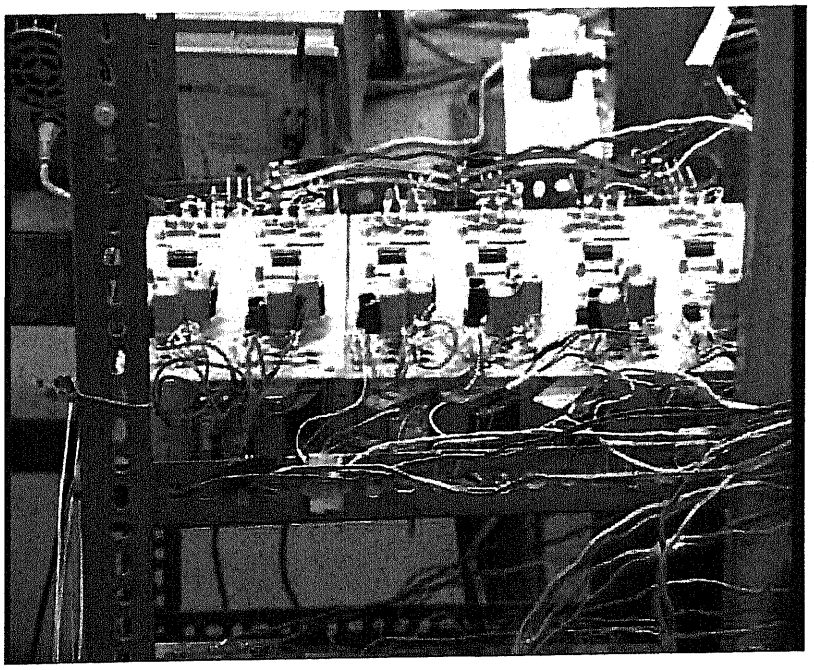


Fig. A.12 Photograph of gate drive circuit and the IGBTs

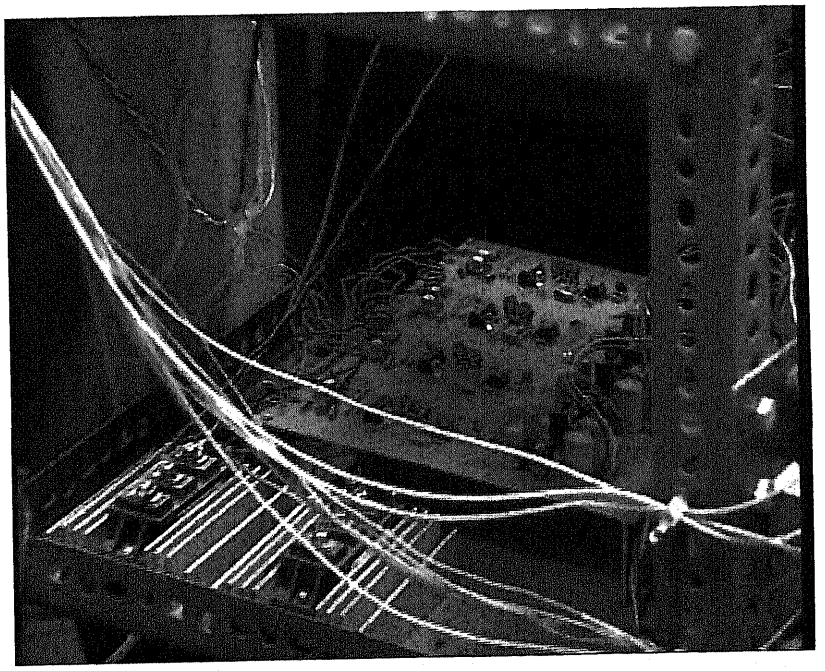


Fig. A.13 Photograph displaying IGBT modules

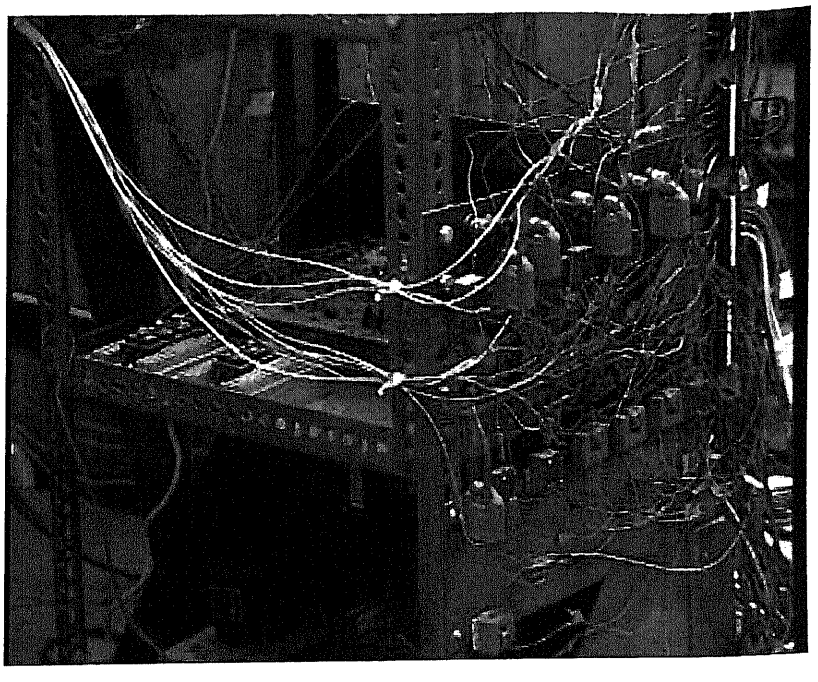


Fig. A.14 Photograph displaying Hall effect voltage and current transducers

Fig. A.15 Photograph displaying various circuits and PC interface

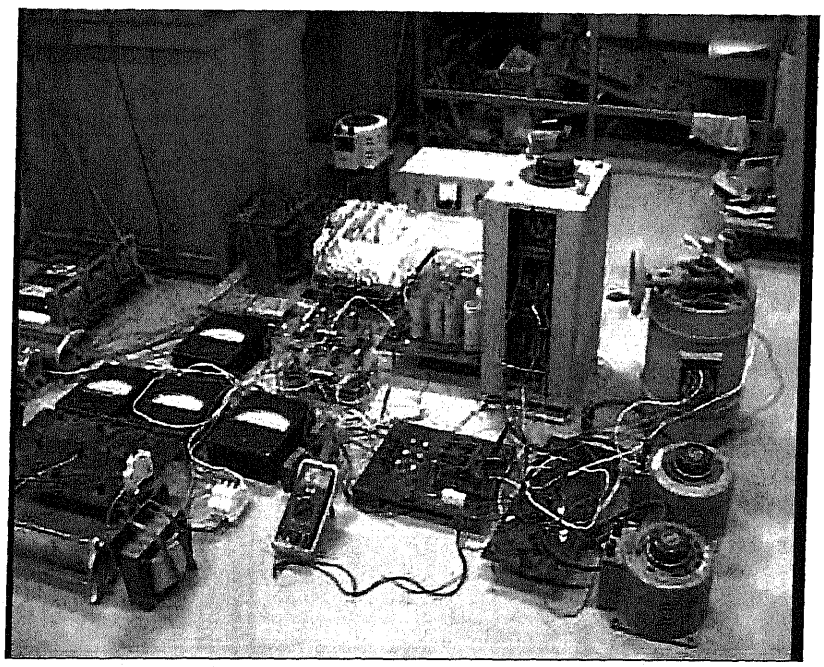


Fig. A.16 Photograph displaying source consisting of three-phase variacs, single phase variacs, phase shifter and measuring circuit

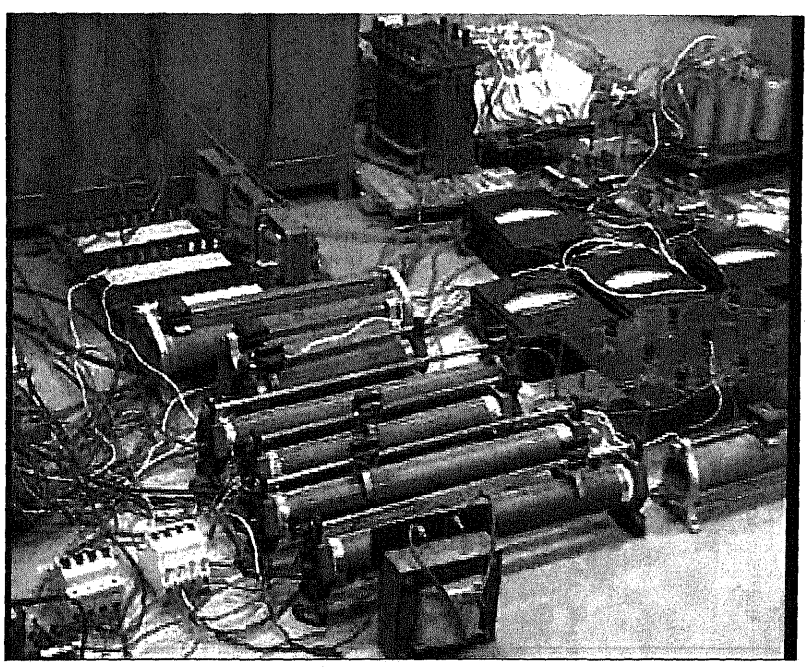


Fig. A.17 Photograph displaying three-phase load circuits, interface inductors, ac filter capacitors

APPENDIX B

DETAILS OF PC INTERFACE DATA ACQUISITION CARD PCI-9118 DG

The PCI-9118 is a advanced performance data acquisition card based on the 32-bit Bus architecture. High performance designs and the state-of-the-art technology make the card idelal for data acquisition and control.

SPECIFICATIONS:

1. Analog to Digital Converter:

- **Converter:** 12 bit ADC using BB ADS7800
- **Input Channels:** 16 channels single ended or 8 differential
- **On chip sample and hold**
- **Input ranges:** (software controlled)

  Bipolar : ±5 V, ±2.5 V, ±1.25 V, ±0.625 V

  Unipolar : 0-10 V, 0-5 V, 0-2.5 V, 0-1.25 V
- **Overvoltage protection:** 70 V peak to peak
- **Accuracy:** 0.01% of FSR ± 1 LSB
- **Input Impedance:** 10,000 MΩ || 6 pF
- **Data Throuhout:** 330 KHz (maximum)

2. Digital to Analog Converter

- **Output Channel:** 2 analog outputs
- **Resolution:** 12 bit
- **Data Format:** Binary format

- **Output Range:** Bipolar: -10 V to +10 V
- **Converter:** AD DA2813
- **Settling Time:** 4.5 μ sec.
- **Linearity:** ±5 ½ bit LSB (Max.), ±1/4 bit LSB (typical)
- **Output Driving:** ± 5 mA

3. **Digital I/O**

Channel: 4 TTL compatible inputs and outputs

APPENDIX C

DETAILS OF HALL EFFECT VOLTAGE AND CURRENT TRANSDUCERS

C.1 VOLTAGE TRANSDUCER

The LV 25-P is a Hall effect transducer for electronic meeasurement of voltages (dc and ac) with isolation between the primary (high power) and the secondary (electronic circuits). For voltage measurements the voltage is collected through external resistance R_o.

SPECIFICATIONS

- **Nominal current :** 10 mA
- **Measuring range:** 0 to ± 14 mA
- **Supply voltages:** +12 V and -12 V
- **Nominal analog output current:** 25 mA
- **Turn ratio:** 2500:1000
- **Overall accuracy at +25° C at ±12 V:** ±0.8% of nominal current
- **Isolation:** between primary and secondary
- **Response time:** Inferior at 500 nS
- **Rise time:** better than 1 μS
- **Bandwidth:** 0-200 kHz (-1dB)

CONNECTION DIAGRAM OF LV 25-P

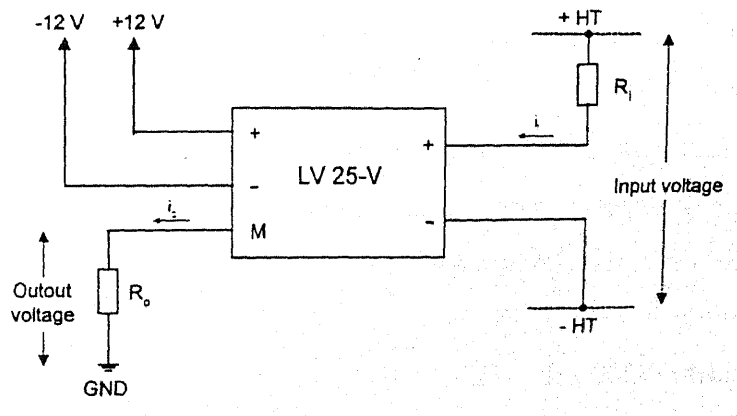


Fig. C.1 Connection diagram for Hall effect voltage transducer

DESIGN EXAMPLE: In the experimental set-up the power voltage is scaled down to 1/100 scale. The input resistance R_i is taken as 50 kΩ. For 100 V peak to peak, the input current i_i is limited to

$$i_i = \frac{v_i}{R_i} = \frac{100}{50 \times 10^3} = 2\,mA$$

The output current i_o is given as

$$i_o = i_i \cdot turn\,ratio = 2.5 \times 2.0 = 5\,mA$$

The output measuring resistance is taken as R_o=200 Ω. Therefore the output voltage is given as,

$$v_o = i_i \times R_o = 5\,mA \times 200\,\Omega = 1000\,mV = 1\,V$$

C.2 CURRENT TRANSDUCER

The LEM Module LA 55-P is a Hall effect current transducer for the electronic mearurement of currents (dc and ac) with isolation between the primary (high power) and the secondary (electronic) circuits.

SPECIFICATIONS

- **Nominal current :** 50 A rms
- **Measuring range:** 0 to ± 70 A at 70° C
- **Supply voltages:** +12 V and -12 V
- **Nominal analog output current:** 50 mA
- **Turn ratio:** 1:1000
- **Overall accuracy at +25° at ±12 V:** ±0.9% of nominal current
- **Isolation:** between primary and secondary
- **Response time:** Inferior at 500nS
- **Rise time:** better than 1 μS
- **Bandwidth:** 0-200 kHz (-1dB)

CONNECTION DIAGRAM OF LA 55-P

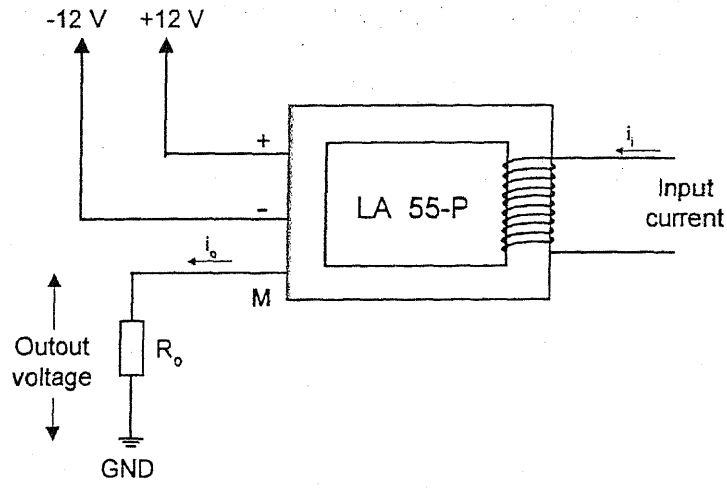


Fig. C.2 Connection diagram for Hall effect current transducer

DESIGN EXAMPLE: In the experimental set 1 A current is converted to 1 V. The design procedure is as follows.Let the input current be i_i. The number of turns on the primary side is 10. Thus ampere turns on the primary side is 10 i_i. The secondary has 1000 turns, therefore the secondary output current is given as

$$i_o = \frac{i_i \times 10}{1000} = 0.01\, i_i$$

This output current is passed through output resistance *Ro* (100 Ω) producing an output voltage v_o according to the following equation

$$v_o = i_o \times R_o = 0.01\, i_i \times 100 = i_i$$

Thus, 1 A input current is represented by 1 V output voltage.